C.R. Communications

CALLPAC TRANSCEIVER PRC 2000

OPERATION & MAINTENANCE HANDBOOK

PN 1238 OCTOBER 89

AMENDMENT RECORD

Amdt No.	Incorporated By	Date	Amdt No.	Incorporated by	Date

OPERATION AND MAINTENANCE HANDBOOK for CALLPAC TRANSCEIVER RT 2000 BA 1172

Contents

Location of Remaining Categories

SAFETY WARNING

RF BURNS

TO AVOID RF BURNS:

ENSURE THAT THE SET IS CORRECTLY EARTHED AT ALL TIMES.

AVOID TOUCHING THE ANTENNA SOCKETS AND EXPOSED ANTENNA ELEMENTS.

ALWAYS USE THE SET IN ITS SATCHEL.

CATEGORY 1

PURPOSE AND PLANNING INFORMATION

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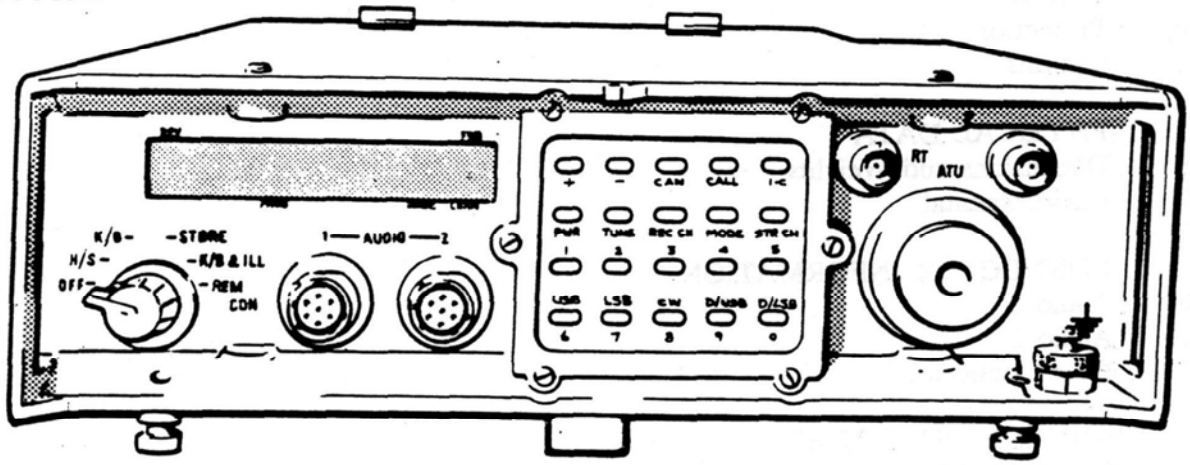

Fig 1.1 Callpac Transmitter/Receiver RT 2000

CATEGORY 1

PURPOSE AND PLANNING INFORMATION

PURPOSE

1 Callpac Transmitter/Receiver RT 2000 is a versatile microprocessor controlled, high frequency (HF) telecommunication transceiver for use in tactical field operations. Within the 1.6 to 30 MHz HF frequency band the transceiver can operate on any one of 284,000 channels spaced at 100 Hz intervals, to provide single side band (SSB) voice or data communication, or continuous wave (CW) Morse communication. In addition to manual channel selection, frequency and mode data for up to 10 channels can be preset in non-volatile memory for immediate recall as necessary.

IDENTITY

2

Manufacturer	:	MEL, Crawley, Sussex
Manufacturer's reference	:	Callpac Receiver/Transmitter RT 2000
MEL type number	:	BA 1172
MEL drawing series	:	9571 111 7200

DESIGN AND PERFORMANCE DATA

Frequency Data

3 General

Frequency Range	:	1.6 to 30 MHz, fully synthesised
No. of channels	:	284,000 in 100 Hz steps
Preset channels	:	10 (frequency and mode) (10 selectable from keyboard) (9 selectable from handset)
Frequency stability	:	1 part in 10^6
Modes of operation	:	Voice SSB: J3E (A3J), upper sideband (usb) and lower sideband (lsb)
		Morse CW: J2A (A2J), usb & lsb, 1 KHz keyed tone A1A (A1) Keyed carrier
		Data: J2D usb & lsb with external modem
Intercom	:	Incorporated into the transceiver. Intercom facilities provided between Audio 1 and Audio 2 connectors. Includes call to remote position

		and radio listen through. Using multiway cable, distances in excess of 200 m.
Antennas	:	2.4 m whip 3.6 m vehicular whip dipole 1/4 wave and 3/4 wave long wire
Antenna tuning	:	Fully automatic, nominal 3.5 seconds tuning time. Manual, silent tune facility available.
Power supply	:	15 V, 4 Ah, NICAD battery or 12 to 24 V vehicle supply with the BA1205.
Battery endurance	:	10 hours (at 1:9 transmit/receive ratio).
Standard	:	'CCIR' or 'FINABEL'

Note: On SSB, 'FINABEL' denotes that the indicated frequency is suppressed carrier; 'CCIR' that the indicated frequency is at approximately the centre of the passband. On CW the indicated frequency is the actual transmitted or received frequency on either 'CCIR' or 'FINABEL'.

Transmitter

4	RF Output Power	:	High: 20 W pep and average Low: 4 W pep and average
	Intermodulation	:	Less than 32 dB relative to pep
	Spurious Emissions		
	In band	:	30 dB below wanted signal
	Out of band	:	60 dB below wanted signal
	Harmonics	:	Radiated Harmonics are typically -40 dB below the fundamental, when using a 2.4 m whip.
	Level control	:	Automatic Level Control (ALC) Automatic Modulation Control (AMC)
	Modulation sensitivity	:	2 to 40 mV emf for full modulation
	Speech Processing	:	VOGAD and peak clipper giving approximately 3 dB peak to mean ratio, employed on voice ssb modes.

Receiver

5	Sensitivity	:	0.6 µV for 10 dB signal to noise ratio
	Selectivity	:	2.9 kHz less than 6 dB 5 KHz greater than 60 dB

Image and IF responses	:	Non-existent (direct conversion used)
Intermodulation response	:	Better than 80 dB at 1 μV emf
Blocking	:	Better than +100 dB at 1 μV emf, for 3 dB degradation in sensitivity
Audio response	:	350 to 3250 Hz
AF output power	:	150 mW into 75 Ω 2 W into 4 Ω external loudspeaker

Protection

6 Transceiver protection :

- antenna, open or short circuit
- high level RF radiation from nearby transmitters
- audio output, short circuit
- reverse polarity of supply voltage

Options

7 CCIR or FINABEL frequency standard
Channel storage protection
Remote control
Amplifier

PHYSICAL DATA

Dimensions and Weights

8 For dimensions and weight of the transceiver and its internal rechargeable battery, refer to Table 1.1.

Table 1.1 Dimensions and Weights

Item	Height (mm)	Width (mm)	Depth (mm)	Weight (kg)
Transceiver RT 2000 (excluding battery)	82.5	272	370	6.65
Rechargeable Ni-Cad Battery	70	234	64	2.0

Environmental

9 Meets the relevant parts of MIL STAN 810C and DEF STAN 07-55

Storage temperature	:	-40 to +70°C
Operational temperature	:	-20 to +60°C
Specification	:	-10 to +60°C
Relative Humidity	:	95% at +40°C
Immersion	:	Sealed to withstand immersion in water to a depth of 1 metre for 2 hours
Shock	:	Withstand drop of 1.0 m onto concrete

CONNECTOR INFORMATION

Audio 1

10 Pin:
- A - Input, 350 to 3250 Hz, 1.5 to 30 mV rms, emf from 600 Ω.
- B - AF Input Earth.
- C - DC Supply. 15 Volts & 150 mA maximum. (Internal and Remote).
- D - AF Output, 350 to 3250 Hz. Preset level typically 3.5 V rms. Impedance levels 4 Ω.
- E - Common Earth
- F - Tx/Rx Switch (Pressel) <140 Ω for Tx, >50k Ω for Rx
  Other impedances will cause radio to change channel if front panel rotary switch is in H/S position.

Resistance F-E	Channel
392	Intercom
523	1
681	2
857	3
1130	4
1470	5
1910	6
2550	7
3570	8
5360	9
--	C (applicable to Clansman)

- G - On/Standby Switch. <100 Ω for Standby, >50k for On.

Audio 2

11 Pin:
- A - As Audio 1
- B - As Audio 1
- C - Store Enable. C-E <100 Ω for enable, >50 kΩ for protection.
- D - As Audio 1
- E - As Audio 1
- F - As Audio 1
- G - Key Morse. <100 Ω for Tx/Tone. >50 kΩ for Tx/No tone. If G is >50k Ω for >300mS, radio returns to receive.

Rear Connector

12 Pin:
- A - External Supply +ve (15 V). 5 A for 20 W, 3 A for 4 W, 1 Amp for Receive only.
- B - Earth.
- C - Transmit high power override. 150 Ω for low power.
- D - Battery direct charge input. 400 mA nominal charge current.

E, F & G - not connected.

SERVICES REQUIRED

Power Supply

13	Internal	:	15 V dc, 4 Ah Ni-Cad rechargeable battery
	External	:	15 V dc, 5 A (11 to 32 V dc vehicle supply with vehicle PSU fitted)
	Consumption	:	60 W max (transmit) 3 W max (receive)

LOGISTIC REQUIREMENTS

Second Line Servicing (Field)

14 Second line servicing requires the use of the special-to-type Test Set, TS 2010 and the Interface Test units listed in Category 5.

ASSOCIATED DOCUMENTATION

Handbooks

15 Callpac PRC/VRC 2000 Operator's Handbook - Manpack Role PN1239

Illustrated Parts Catalogue PN1553

CATEGORY 2

OPERATING INFORMATION

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CHAPTER 2.1

CONTROLS AND INDICATORS

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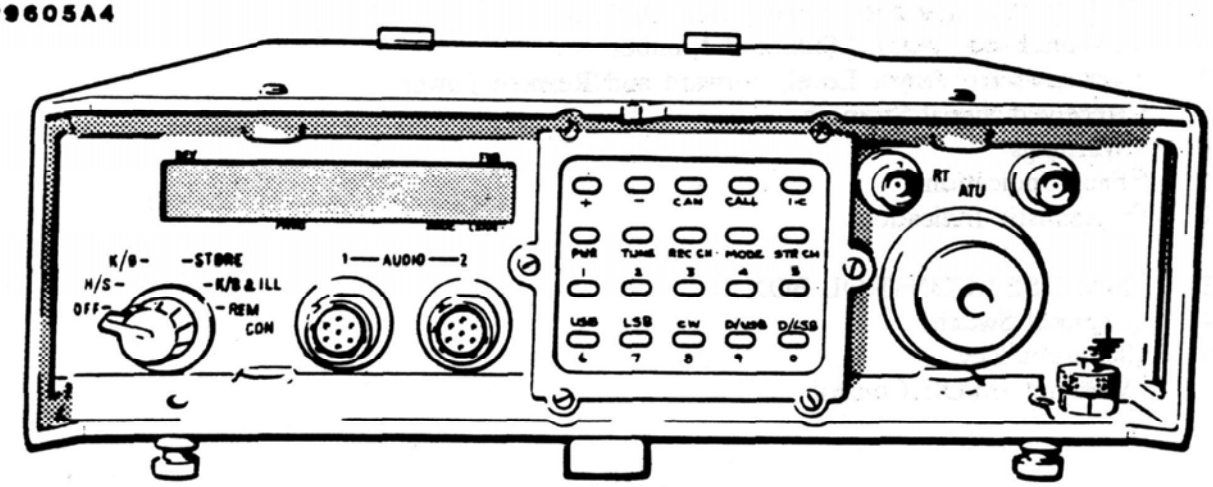


Fig 2.1.1 RT 2000 Controls and Indicators

CHAPTER 2.1

CONTROLS AND INDICATORS

INTRODUCTION (Fig 2.1.1)

1 All primary control operations, for HF Radio Communication System VRC 2000, are carried out at the RT 2000 transceiver front panel which also provides all visual indications. The front panel incorporates the following:

(a) Rotary Switch
(b) Keyboard
(c) Liquid Crystal Display

ROTARY SWITCH

2 The six position rotary selection switch is used to determine the system working condition. Any of the following settings can be made:

OFF	Radio powered off. Stored information is retained. At power on, previous settings are restored and built-in options are displayed for a few seconds (para 5).
H/S	Control of on/off, volume and channel selection (1 to 9) is passed to the handset/control box. Keyboard inactive except for volume ('+' and '–') and CALL keys.
K/B	Control is passed to the keyboard. All keys are active.
STORE	Channel data can be read, over-written or erased. A warning tone is generated.
K/B & ILL	As for K/B; also display is illuminated for 10 seconds after selection and on subsequent key-presses. Display remains illuminated throughout the transmit period if transmission commences whilst display is lit.
REM CON	Full remote control operation of RT 2000 possible if option is fitted. A fast intermittent tone is generated and ILL(egal) is displayed if the option is not fitted (para 5).

KEYBOARD

3 The 20 keys of the multifunction keyboard are enabled in the K/B positions of the rotary switch. They are used by the operator, to perform control functions by individual or combined key selection as follows:

'+' & '–'	Used either alone to increase ('+') or decrease ('–') volume, or with the numeric keys to increment frequency, with the PWR key to select transmitter power, or with the TUNE key to tune the antenna manually.

CANCEL	Cancels completed or incorrect entries through the keyboard, returning the display to the frequency/mode of the selected channel.
CALL	Initiates transmission of a 2 second (approximately) burst of two-tone call signature. Can also be used to initiate fine antenna tuning, which once completed is followed by a 2 second (approximately) call tone transmission.
IC	Selects intercom working. RF transmission is inhibited and receiver audio is attenuated 10dB below intercom level.
PWR	Used with the '+' and '–' keys. Operation of this key displays current transmitter power selection on the LCD and programmes the '+' and '–' keys for selection of transmitter power.
TUNE	Used with the '+' and '–' keys. Operation of this key clears the frequency/mode data from the LCD and displays a single digit representing received signal strength. The '+' and '–' keys are operated to optimise signal strength.
REC CH	Used with the numeric keys to recall any one of the 10 stored channels. Operation of this key precedes selection of the channel number.
MODE	Used in K/B working to alter temporarily the mode of the currently selected channel or, when rotary switch is set to STORE, to store a mode permanently.
STORE CH	Used with the numeric and MODE keys. Operation of this key enters frequency/mode data into the store of selected channel.
0 to 9	Used to enter numeric data.

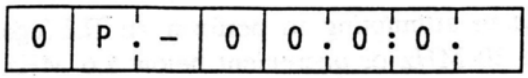
LIQUID CRYSTAL DISPLAY

4 The eight character alphanumeric liquid crystal display (LCD) provides the operator with visual indication of the following system parameters:

(a) RT 2000 configuration and fitted options
(b) Channel frequency, mode and number
(c) Selected transmission power level
(d) Measured forward and reverse power
(e) Received signal strength
(f) Warnings
(g) Fault indications
(h) Diagnostic indications

RT 2000 Configuration and Fitted Options

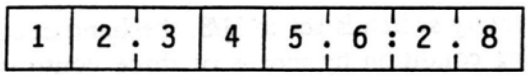
5 When the transceiver rotary switch is moved from OFF to any of the remaining five positions the OP(tion) display indication is presented for a few seconds. The right hand four digits, in the diagram, can each be 0 or 1 dependent on fitted options. The display is interpretated as follows:



Left hand digit	:	0 Amplifier ROM not fitted 1 Amplifier ROM fitted
Second digit	:	0 Remote Control ROM not fitted 1 Remote Control ROM fitted
Third digit	:	0 Store Protection active 1 Store Protection inactive
Right hand digit	:	0 FINABEL frequency standard 1 CCIR frequency standard

Channel Frequency, Mode and Number

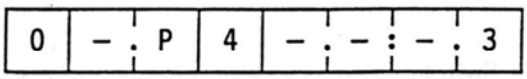
6 This is the normal display indication which appears during receive working unless displaced as a result of certain keyboard operations or as a result of fault conditions. In the example given RT 2000 is operating on 12.3456 MHz, Mode 2, Channel 8.



Transmission Power Level, Forward and Reverse Power

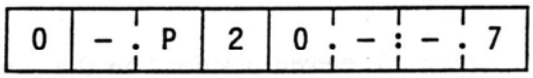
7 During transmit working the normal display indication should be one of two power formats.

4 Watts



or

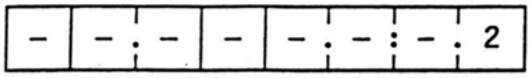
20 Watts



8 The left hand digit, in both instances, is variable 0 to 9 and indicates Reverse Power. The right hand digit similarly indicates Forward Power. P indicates Power format and the digits attached designate low power working (4 watts) or high power working (20 watts).

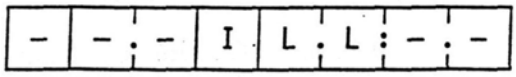
Received Signal Strength

9 Received signal strength is indicated by the right hand digit on a scale of 0 to 9, the remaining characters being blank, when manual tuning is taking place.



Warnings

10 ILL is displayed when attempting to perform an ILL(egal) operation. Attempting to increment frequency above 30 MHz or decrement below 1.6 MHz, attempting to tune with the 'U' link removed or the wrong type of antenna connected, or to select remote control for a system which does not have this option fitted, will produce the ILL indication.



Fault Indications

11 Any indication which does not accord with that specified for the current condition is interpreted as a fault indication. Refer to the appropriate routines tabulated in Chapter 2.3.

Diagnostic Indications

12 Standard indications are anticipated for functional and performance routines. Chapter 2.3 recommends remedial action, which may be undertaken by the operator, or return of equipment to the Field Maintenance workshop according to diagnostic indications observed.

HANDSET/CONTROL BOX

13 When the transceiver rotary switch is set to H/S, the handset/control box enables operator selection of transceiver working condition by means of three controls:

(a) Channel switch
(b) Transmit key (pressel)
(c) Volume, on/off control

Note: The handset/control box connected to the AUDIO 1 socket has control priority.

Channel Switch

14 There are eleven positions on the rotary Channel Switch. Ten positions enable operator selection of any one of the nine preset working Channels (1 to 9), or selection of intercom working (I). Position (C) of the Channel Switch is for Clansman application only.

Transmit Key

15 The transmit key is functional when the working channel has been preset for transmit/receive operation (Mode 1 to 5) and when intercom working has been selected. The key is of the 'press to transmit' type, initiating transmit/receive switching and, when appropriate, automatic antenna tuning.

Volume, On/Off Control

16 The volume, on/off control operation is conventional with 'OFF' referring to RT 2000. When the handset/control box is connected to the AUDIO 1 socket, with the volume control rotated fully counter-clockwise to the OFF position, the transceiver is powered down. This

condition is called Standby to differentiate between the OFF position at the transceiver front panel rotary switch.

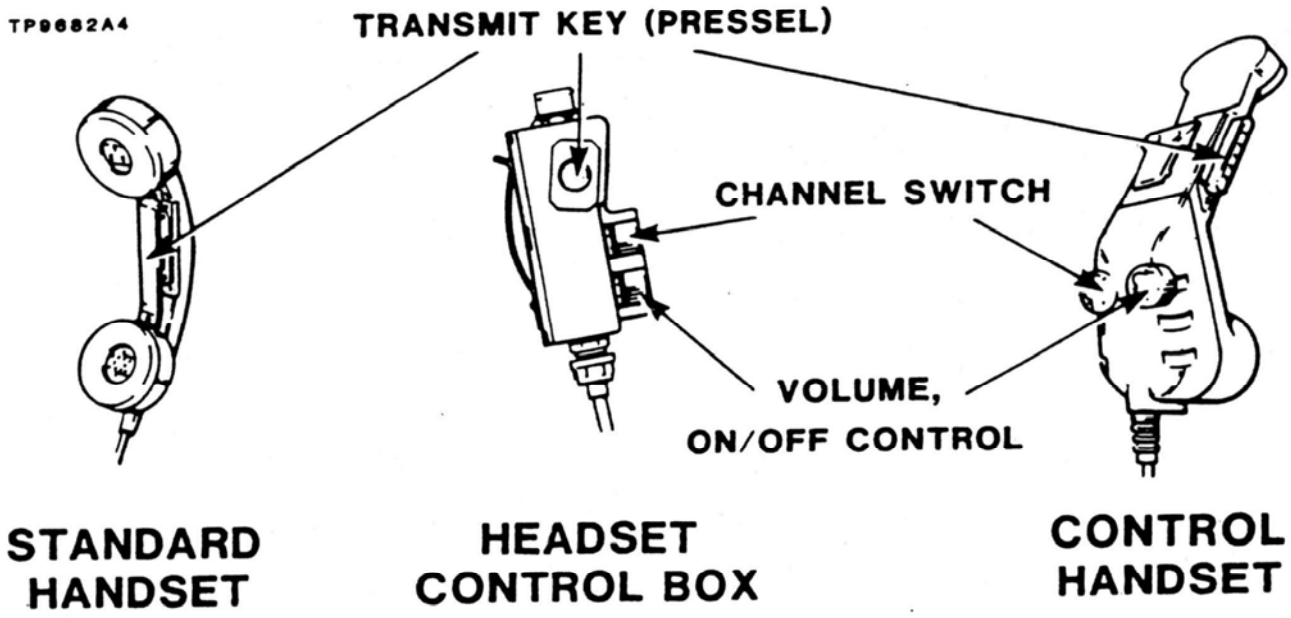


Fig 2.1.2 Handset/Control Box

CHAPTER 2.2

USE OF CONTROLS

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CHAPTER 2.2

USE OF CONTROLS

INTRODUCTION

1 The operating procedures for Callpac HF Communication System require initial pre-selections to be made using RT 2000 front panel controls. Data inserted at this stage can be stored, even with the transceiver powered down, so that subsequent operation normally entails only selection of working condition and use of the Handset/Control Box. The procedures are considered here under the following headings:

(a) Keyboard operations
(b) Operations with preset channels

SPECIAL TOOLS

2 Memory Store Key BA 1233

KEYBOARD OPERATIONS

3 Most keyboard entries are made with the transceiver rotary switch set to K/B or K/B & ILL. The following paragraphs indicate when other settings are possible or mandatory. Use of the CANCEL key may not always be necessary, this depends on the function previously in use. The instructions given here assume that the previous function is not known.

Cancelling an Entry or Function

4 To cancel a complete or partially complete entry or negate a function, press CANCEL. The display will show the frequency and mode of the most recently entered channel, and the equipment is set to receive.

Setting Volume

5 This operation can be performed with the rotary switch set to H/S, K/B or K/B & ILL. At switch-on an intermediate volume level is set. To increase level press '+'. To decrease level press '–'. Release key at desired level.

Manual Antenna Tuning

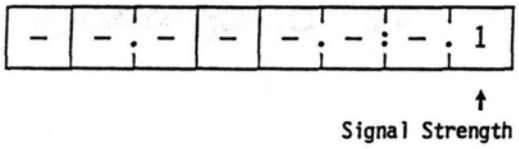
6 This operation can be performed only when the Antenna Tuning Unit (ATU) is in use, ie 'U' link connected.

(1) Set rotary switch to K/B or K/B & ILL.

(2) Press CANCEL.

(3) Verify that 'U' link is connected.

(4) Press TUNE and observe the display.



(5) Operate the '+' key (increase tune frequency) or '–' key (decrease tune frequency) for maximum received signal strength number on the display, or for best signal volume in the earpiece.

Note: At low signal levels the noise of the internal tuning motor may mask the audio signal; in this instance operate the '+' or '–' keys momentarily and listen for improved receiver performance between key operations.

(6) When satisfied that tuning is optimum, press CANCEL key to return to normal operation.

Automatic Antenna Re-tuning

7 When transmit/receive channels (modes 1 to 5) are selected, the antenna can be re-tuned at any time.

(1) Press CANCEL

(2) Press STORE CH

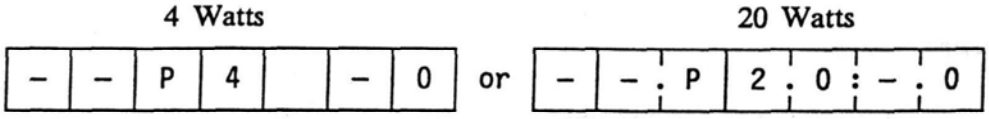
(3) Momentarily operate pressel on the handset/control box, or press CALL button to initiate antenna re-tune.

Selecting Transmitter Power Level

8 The power level may be set to 4W or 20W.

(1) Press CANCEL

(2) Press PWR and observe display:



(3) Press '+' to increase power, '–' to decrease power.

(4) Press CANCEL to re-display frequency.

Recalling a Stored Channel

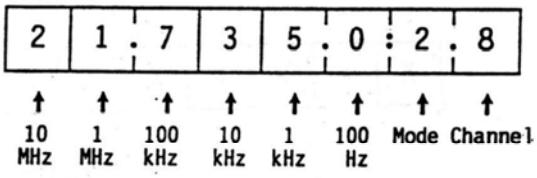
9 This operation achieves recall of previously stored mode and frequency data associated with the channel number concerned.

(1) Press CANCEL

(2) Press REC CH

(3) Press numeric key corresponding to channel number required; observe display:

(Typical Display)



(4) Momentarily operate pressel to tune antenna; wait for tone to cease.

Notes:

(a) Auto antenna tune is inhibited if receive only channel (modes 6, 7, 8, 9 or 0) is selected; use manual antenna tune procedure, para 6.

(b) During receive, the display is as shown in (3) above. During transmit, the display changes to one of the power formats (Chap 2.1, Para 7).

(c) Selection of a channel which does not contain previously stored frequency and mode data automatically presents a frequency of 4 MHz, mode 1.

Entering a Mode

10 Non-stored information is lost when new data is entered or another channel is selected. Provided channels are not changed, the information is retained if the transceiver is switched off.

(1) Check rotary switch is set to K/B or K/B & ILL.

(2) Press CANCEL. The current channel data will be displayed.

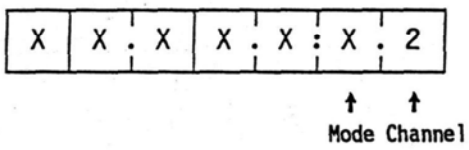
(3) Press MODE.

(4) Press numeric key representing the required mode (Table 2.2.1).

Table 2.2.1 Mode Selection

Mode	Mode digit	
	Tx/Rx	Rx
USB - Voice with speech processing or Key	1	6
LSB - Voice with speech processing or Key	2	7
CW - Key	3	8
USB - no speech processing	4	9
LSB - no speech processing	5	0

(5) Observe display:



(6) Press STORE CH to implement operation of the new mode on the selected channel. Check channel number on display changes to –, indicating non-stored information.

Entering a Frequency

11 Non-stored information is lost when new data is entered or another channel is selected. Provided channels are not changed, the information is retained if the transceiver is switched off.

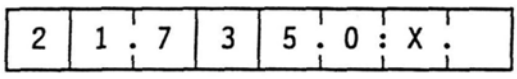
(1) Check rotary switch is set to K/B or K/B & ILL.

(2) Press CANCEL.

(3) Enter frequency by pressing numeric keys in descending order of frequency; observe display.

eg to enter a frequency of 21.7350 MHz press '2','1','7','3','5','0'.

Note: It is essential to include the final '0' as the frequency digits enter from the 100 Hz digit position and jump across one place as each new digit is entered.



(4) Press STORE CH key to implement operation at the new frequency. Check channel number on display changes to –, indicating non-stored information.

Note: If the frequency entered is outside the permitted range, the display shows 'ILL'; press CANCEL key and enter correct frequency.

(5) Momentarily operate the transmit pressel or press CALL button to tune the antenna (Modes 1 to 5 only).

Incrementing Frequency

12 The frequency may be changed by a single increment or by automatic repetition of an increment.

(1) Press CANCEL

(2) Enter frequency increment by pressing numeral keys in descending order of frequency; observe display:

eg to enter a frequency increment of 10 kHz, press '1', '0', '0'.

Note: It is essential to include the final '0' as the digits enter from the 100 Hz digit position and jump across one place as each new digit is entered.

(3) To increase frequency press '+' key.

(4) To decrease frequency press '–' key.

Note: Momentary operation of the '+' or '–' keys, steps the frequency of the selected channel by one incremental step at a time. If the chosen key is pressed and held, frequency automatically steps at an increasing speed, the starting interval being approximately 2 seconds. Maximum speed is reached after 10 steps.

Storing a Channel

13 Mode and frequency data may be allotted a channel number and stored for future recall.

(1) Plug the Memory Store Key BA 1233 into the Audio 2 connector.

(2) With rotary switch set to K/B or K/B & ILL enter mode and or frequency data as required (refer to para 10 and 11) but do not press STORE CH key.

(3) Set rotary switch to STORE.

Note: A pulsating audio tone will be heard in the handset earpiece.

(4) Press STORE CH

(5) Press numeric key representing the number of the channel in which the information is to be stored.

(6) Set rotary switch to K/B or K/B & ILL as required.

(7) Programme as many channels as required; refer to para 14, to check validity of channels.

(8) Remove the Memory Store Key from the Audio 2 connector.

Examining Stored Channels

14 The following operations permit examination of all channel stored information, whilst maintaining a listening watch on a selected channel; transmission is inhibited whilst examination is in progress.

(1) Set the rotary switch to STORE.

Note: In addition to the normal received audio, a pulsating tone signal will be heard in the earphone.

(2) Press the REC CH

(3) Press numeric key corresponding to the channel to be examined.

(4) Examine the display; a blank display indicates that nothing is stored in that channel.

(5) If further channels are to be examined, repeat from operation (3).

(6) When examination is complete, reset rotary switch to K/B or K/B & ILL.

Erasing Memory

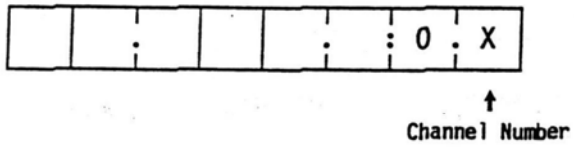
15 The following procedure is not considered a standard operator function but it provides an emergency security feature in the event of imminent equipment capture.

(1) Set the rotary switch to the STORE position.

(2) Press any three keys simultaneously.

Notes:

(a) Stored and non-stored information for all operational channels is erased. The display shows the option format for a few seconds and then changes to the following display.



(b) When the rotary switch is set to an operational position, all channels will display 4 MHz, Mode 1.

Calling a Remote Station or Second Level Operator

16 The call facility generates a two-tone audio signal lasting 2 seconds. This will be heard in locally-connected earphone(s) and at the remote station if a transmit mode is selected.

(1) Check that rotary switch is set to H/S, K/B or K/B & ILL.

(2) Press CALL. A power format is displayed (Modes 1 to 5 only) and the call signal is generated. On release the set reverts to receive.

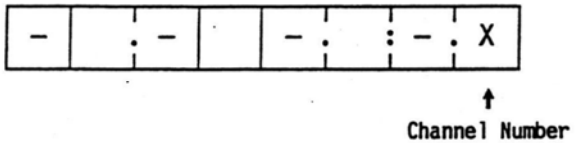
(3) To call second local operator only, select intercom (see below) and press CALL.

Selecting Intercom Working

17 The intercom facility permits conversation between two operators without RF transmission. Received audio remains audible at reduced volume whilst intercom is selected.

(1) Check that rotary switch is set to K/B or K/B & ILL

(2) Press IC. The display will show:



(3) Press CANCEL to revert to normal operation

OPERATION WITH PRESET CHANNELS

18 The controls on the handset/control box provide functions as follows:

Switched Volume control - Listening level control, ON/OFF (standby) switching of RT 2000

Channel selection switch - Selection of Channels 1 to 9 Selection of intercom working

Pressel - Tx/Rx selection, Auto-tune of VRC 2000 antenna (Modes 1 to 5).

Setting Listening Level

19 Rotate volume control clockwise to increase volume.

Switching ON/OFF

20 Rotate volume control fully counter-clockwise to switch to standby; the transceiver rotary switch overrides the setting of the volume control switch.

Selection of Channel and Intercom Working

21 Rotate channel switch to required position. A warning tone is generated in the earphone and after a brief delay intercom working is presented. Transmission is inhibited during the changeover. If intercom has been selected at the transceiver keyboard transmission is inhibited on a selected channel but received signals are heard, attenuated, in the earphone.

Transmit/Receive and Auto-tune

22 Operate the pressel switch to transmit and release to receive. Operation for the first time after selection of any transmit only channel (Modes 1 to 5) initiates auto-tune during which a warning tone is heard in the earphone.

CHAPTER 2.3

OPERATOR TEST AND MAINTENANCE

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Tables

Illustrations

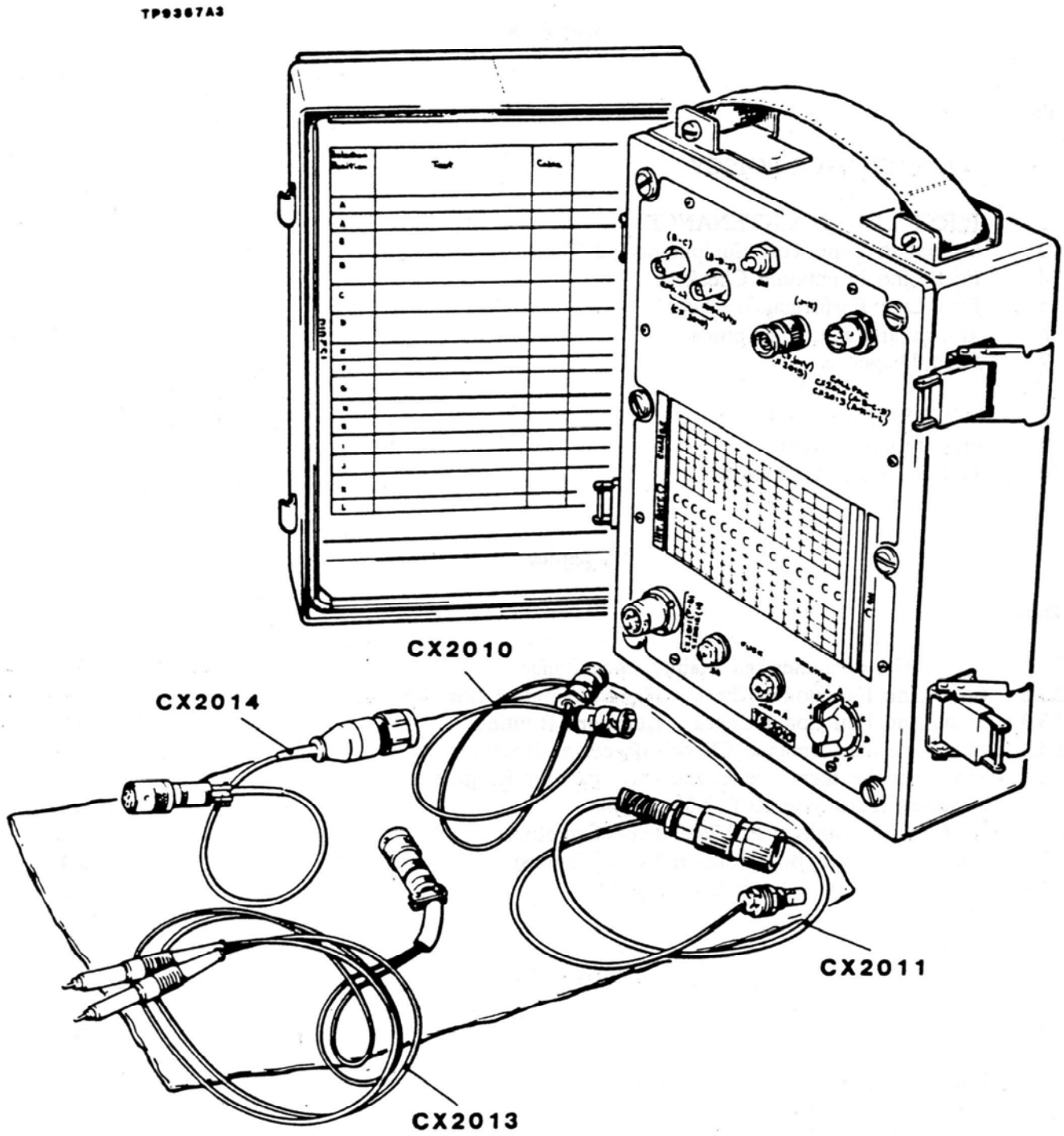


Fig 2.3.1 Test Set TS 2010

CHAPTER 2.3

OPERATOR TEST AND MAINTENANCE

MAINTENANCE POLICY

1 The maintenance policy adopted for Receiver/Transmitter RT 2000 depends upon the organisational requirements of the user. The recommended maintenance policy shown in Table 2.3.1 is for user guidance.

Table 2.3.1 RT 2000 Recommended Maintenance Policy

Level	Carried Out by	Description
First-line Functional Check	Operator	Enables operator to check correct functioning of the system by use of a Handset/Control Box Routine and a Keyboard Routine. This is a simple check requiring no special test equipment.
First-line Performance Check	Operator or technician	Enables operator or technician to check the performance of the radio, by use of a Receiver Routine and a Transmitter Routine. Both routines are carried out with the transceiver closed using the special-to-type Test Set TS 2010.

FIRST LINE MAINTENANCE

2 Routine operator maintenance is confined to maintaining equipment cleanliness and battery charging. When a deterioration in operational performance is suspected, functional and performance checks are performed as an aid to identifying the cause. To enable these checks to be made by an operator, with no technical knowledge of the system, four test routines are provided as follows:

(a) Handset/Control Box Routine - Table 2.3.2
(b) Keyboard Routine - Table 2.3.3
(c) Receiver Routine - Table 2.3.4
(d) Transmitter Routine - Table 2.3.5

Special to Type Test Equipment and Tools

3 All routines are performed with the transceiver closed. Routines (a) and (b) use normal system facilities, routines (c) and (d) require the use of the following items of test equipment:

(a) Test Set TS 2010
(b) Memory Store Key BA 1233
(c) Dummy Antenna

TP9368A4

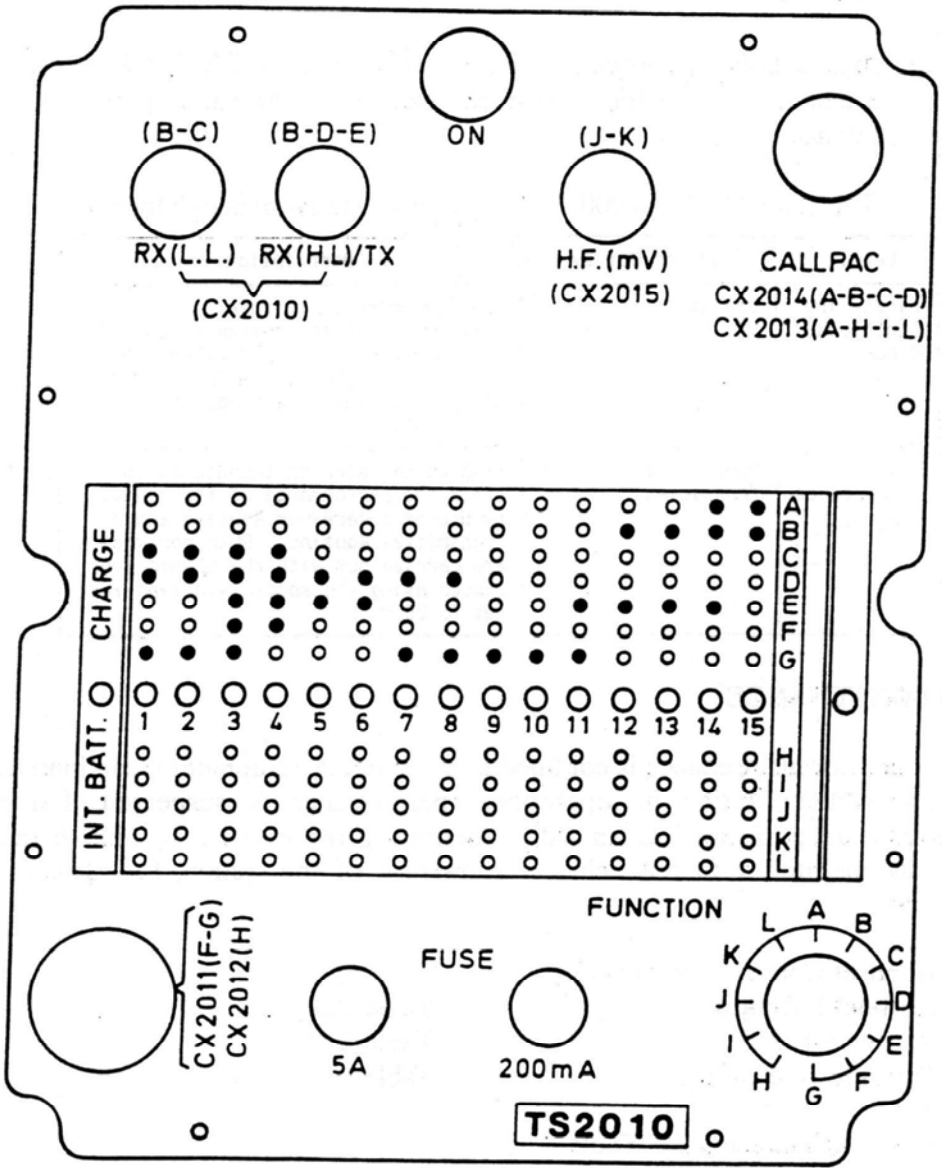


Fig 2.3.2 Test Set TS 2010 Front Panel

CAUTION: **RT 2000 must NOT be opened**

First Line Functional Check

4 The functional check is made by following Handset/Control Box and Keyboard routines described in Tables 2.3.2 and 2.3.3.

First Line Performance Check

5 The performance check is made by following Receiver and Transmitter routines described in Tables 2.3.4 and 2.3.5.

Alarms and Fault Symptoms

6 Table 2.3.6 describes RT 2000 alarms, causes and actions to be taken. Table 2.3.7 lists fault symptoms and actions to be taken.

Fault Diagnosis

7 Guidance to the diagnostic interpretation of Handset/Control Box and Keyboard Routine indications is provided in Tables 2.3.8 and 2.3.9.

TEST SET TS 2010 (Fig 2.3.1 to 2.3.4)

8 Special-to-type Test Set TS 2010 (Fig 2.3.1) is a self contained battery powered unit for transceiver RT 2000 performance testing. The front panel (Fig 2.3.2) carries a biased off power switch, a rotary FUNCTION switch, a light emitting diode (LED) display and five test sockets. The test set lid contains all necessary test cables and a list (Fig 2.3.3) showing the correlation between tests, cables and test sockets. Fig 2.3.4 shows a typical test configuration.

Preparation For Use

9 Prior to conducting transceiver test routines a check must be made on the test set battery by performing the following procedure:

(1) Remove test set lid.

(2) Press power switch (biased off).

(3) Observe ON LED. Flashing or failure to light indicates the need to recharge the test set battery.

(4) Release power switch.

Test Set Battery Charging

CAUTION: Never recharge battery unless necessary.

10 The 12 V nickel cadmium battery is charged using an internal charger and a dc supply in the range 11 to 32 V. To charge the battery carry out the following procedure:

(1) Connect cable CX 2013 to the CALLPAC socket on the test set.

(2) Set the test set FUNCTION switch to Position H.

(3) Connect the free ends of Cable CX 2013 to the dc supply, red to positive, black to negative. The INT BATT LED should illuminate.

(4) Allow up to 14 hours for full charge.

Selection Position	Test	Cable	To
A	DC Voltmeter, 2 to 16 V : 1 V/step	CX2013	Circuit to be measured
A	Battery Check	CX2014	Callpac Audio 1
B	RX(LL) : S + N	CX2014 CX2010	Callpac Audio 1 Callpac BNC-RT
B	Rx(HL) : S + N	CX2014 CX2010	Callpac Audio 1 Callpac BNC-RT
C	Rx(LL) : N	CX2014 CX2010	Callpac Audio 1 Callpac BNC-RT
D	Rx(HL) : N	CX2014 CX2010	Callpac Audio 1 Callpac BNC-RT
E	Tx Power 4 W or 20 W	CX2010	Callpac BNC-RT
F	Rx Battery Current, 150 to 500 mA : 25 mA/step	CX2011	Callpac Fuse Holder
G	Tx Battery Current, 1.5 to 5.0 A : 0.25 A/step	CX2011	Callpac Fuse Holder
H	TS 2010 Battery Charge	CX2013	DC, 11 to 32 V
H	DC Current, 30 to 100 mA : 5.0 mA/step	CX2013	Callpac modules
I	DC Voltmeter, 16 to 30 V : 1 V/step	CX2013	Circuit to be measured
J	HF mV meter, low level : -10 to +2 dBm	CX2015	Callpac modules
K	HF mV meter, low level : -2 to +13 dBm	CX2015	Callpac modules
L	Continuity, 0-1400 ohms : 100 ohms/step	CX2013	Circuit to be measured

Fig 2.3.3 Test Set TS 2010 Test Table

Table 2.3.2 First Line Functional Check - Handset/Control Box Routine

STEP	PROCEDURE	REQUIRED INDICATION
	Note: Throughout the following tests, the combination of Standard Handset and Headset Control Box, or the Control Handset will be referred as H/S.	
1	Set transceiver function switch to OFF, connect H/S to AUDIO 1 socket, check that standard adaptors and connectors are correctly fitted.	
2	Check antenna free of damage and correctly fitted.	
3	Set H/S volume control to mid-range.	
4	Set transceiver function switch to H/S.	
5	Observe transceiver display and listen at phone Observations: (a) Display shows Option Format for 2 seconds then reverts to Normal Display Format. (b) Phone silent for 2 seconds then presents received signal or noise. (c) If display shows BA and phone presents intermittent tone, Charge or change battery See also Table 2.3.8. (d) If display shows P4 or P20 H/S is connected to AUDIO 2 and switched OFF. Transfer to AUDIO 1, refer to Step 4.	0 P . - X X . X : X . Option Format (X = 0 or 1) X X . X X X . X : X . X FREQUENCY MODE CHANNEL Normal Display Format (X = 0 to 9)
6	At transceiver: push and hold '+' push and hold '-' push + and release at suitable audio level. Note: If volume unvaried, change transceiver.	PHONE Volume increases Volume decreases Volume increases
7	At transceiver push CALL, observe display. Notes: (a) Channel selected at H/S must have preset mode in range mode 1 to mode 5. (b) X at left smaller number than X at right, if not check antenna fittings, change transceiver (See also Table 2.3.8)	X - . P 2 0 . - : - . X High Power Format X = 0 to 7 OR X - . P 4 - . - : - . X Low Power Format X = 0 to 7 Reverts to Normal Display Format PHONE Single note tone during Auto Tune reverts to two note tone or Two note tone immediately if tuning previously accomplished
8	Operate pressel, speak into handset, observe display and listen for own voice in earpiece. Not applicable to mode 3, see step 10. Note: Step 7 notes (a) and (b) apply.	High or Low Power Format

Table 2.3.2 First Line Functional Check - Handset/Control Box Routine (Cont.)

STEP	PROCEDURE	REQUIRED INDICATION
9	Release pressel and check that display reverts to normal display format.	
10	If display shows mode 3 - go to step 11, else go to step 13.	
11	Operate pressel, observe display and listen for continuous tone.	High or Low Power Format
	Note: X at left much smaller number than X at right	
12	Release pressel and check that display reverts to normal display format and that RX signal or noise is audible.	
13	At H/S, Change Channel, observe display.	Normal Display Format Intermittent tone audible during Channel change
	Note: If preset frequency for channel selected is in different frequency band, mechanical sound of tuning apparent at transceiver.	
14	Set transceiver function switch to OFF.	

Table 2.3.3 First Line Functional Check - Keyboard Routine

STEP	PROCEDURE	REQUIRED INDICATION
1	Set transceiver function switch to OFF. Ensure no anciliaries connected to AUDIO 1 or AUDIO 2 sockets. Remove 'U' link and disconnect Antenna.	
2	Conduct following Steps in sequence. For any erroneous indication refer to Table 2.3.9.	
	Test 1	
3	Set transceiver function switch to H/S, observe indications. Note: For explanation of Formats refer to Step 6 of Table 2.3.2.	Option Format for 2 seconds Reverts to Normal Display Format
	Test 2	
4	At transceiver insert 'U' link across RT and ATU connectors, observe indications.	Option Format for 2 seconds Reverts to Normal Display Format
5	Remove 'U' link, observe indications (leave disconnected).	Option Format for 2 seconds Reverts to Normal Display Format
	Test 3	
6	Set transceiver function switch to K/B.	
7	Push '1' six times, observing display after each push. Note: The value of Mode digit X is to be ignored through Steps 7 to 11.	. . .1 : X . . . 1.1 : X . . . 1 1.1 : X . . .1 1 1.1 : X . . 1.1 1 1.1 : X . 1 1.1 1 1.1 : X .
8	Push '2' six times, observing display after each push.	First push 1 1.1 1 1.2 : X . Sixth push 2 2.2 2 2.2 : X .
9	In turn, push all digit keys from 3 to 9, six times observing frequency display incrementing as in Steps 7 and 8	
10	Push '0' five times, observe display.	9 0.0 0 0.0 : X .
11	Push '0', observe display.	. . . . : X .
12	Push MODE	. . . . : .

Table 2.3.3 First Line Functional Check - Keyboard Routine (Cont.)

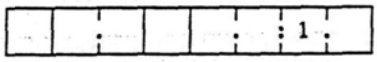
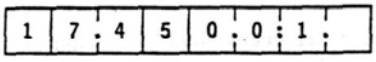
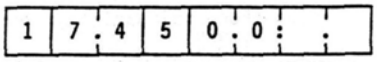
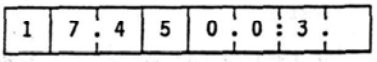
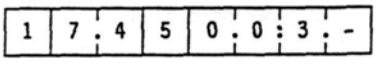
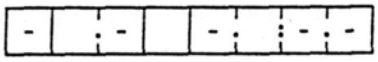
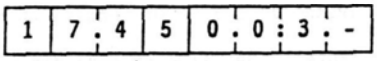
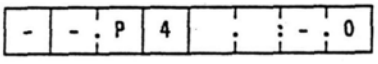
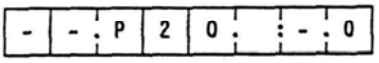
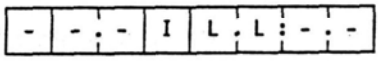
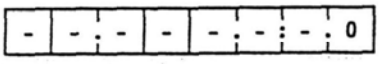
STEP	PROCEDURE	REQUIRED INDICATION
13	Push '1'	
	Test 4	
14	Enter a frequency of 17.450.0 MHz	
15	Push MODE	
16	Push '3'	
17	Push STORE CH	
	Note: (a) Observe appearance of hyphen. (b) Listen for mechanical tuning.	
	Test 5	
18	Push IC	
19	Push CANCEL	
	Test 6	
20	Push PWR	
	Notes: (a) Push '+' to change from Low Power Format to High. (b) Push '-' to change from High Power Format to Low.	or 
21	Push CANCEL and check display reverts to normal display format.	
	Test 7	
22	Push TUNE, observe Illegal format	
23	Insert 'U' link, observe option format reverting to normal display format after 2 seconds.	
24	Push TUNE, observe Tune format.	
25	Place the ear close to transceiver case, maintain '+' key pressed, listen to mechanical sound of ATU tuning for 6 to 8 seconds.	
26	Repeat procedure of Step 25 with '-' key pressed.	
27	Push CANCEL and check display reverts to normal display format.	
28	Remove 'U' link, observe display of Option format reverting to normal display format after 2 seconds.	

Table 2.3.3 First Line Functional Check - Keyboard Routine (Cont.)

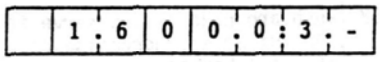
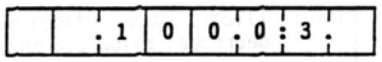
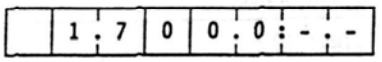
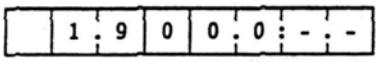
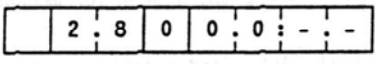
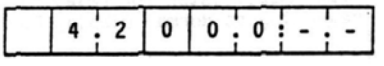
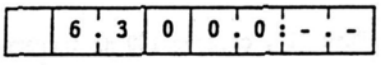
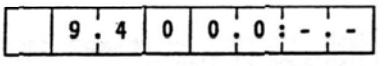
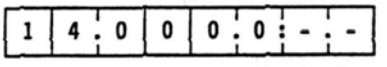
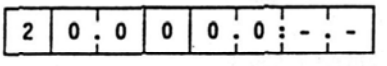
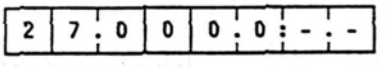
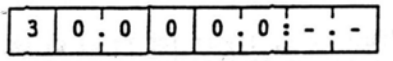
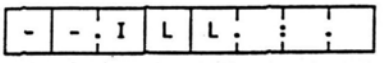
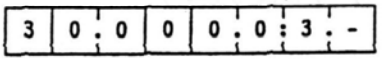
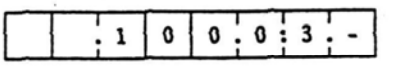
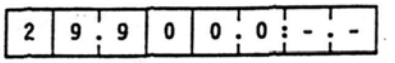
STEP	PROCEDURE	REQUIRED INDICATION
	Test 8	
29	Enter 1.600.0	
	Push STORE CH, observe display, listen for mechanical tuning	
30	Push CALL, observe Power format reverting to Normal display format when CALL complete.	
31	Repeat Step 30 listening for relay operation.	
	Test 9	
32	Enter 100.0, observe 100 kHz increment displayed.	
33	Push '+', observe frequency displayed advances by 100 kHz from that displayed at Step 29.	
34	Push and hold '+', observe frequency displayed advances by 100 kHz at an increasing rate. Note that band changes take place and mechanical sound will be heard at eight frequencies shown in right hand column.	       
	Notes: (a) Maximum frequency displayed is 30 MHz.	
	(b) Illegal format displayed as frequency attempts to increment beyond 30 MHz.	
35	Release '+'	Normal Display Format
	Push CANCEL	
	Note: PH appearing on the display, at any time, indicates loss of phase lock. The transceiver cannot be used at any frequency at which this occurs.	
36	Enter 100.0, observe 100 kHz increment displayed.	
37	Push '-', observe frequency displayed decreases by 100 kHz on that displayed at Step 35.	

Table 2.3.3 First Line Functional Check - Keyboard Routine (Cont.)

STEP	PROCEDURE	REQUIRED INDICATION
38	Push and hold '-', observe frequency displayed decreases by 100 kHz at an increasing rate. Listen for mechanical sound of band changes.	29.800.0:-.- down to 1.600.0:-.- then --.-IL.L:-.-
	Note: Illegal format displayed as frequency attempts to decrement below 1.6 MHz.	1.600.03.-
39	Push CANCEL	
	Test 10	
40	Enter 4.499.9	4.499.93.
41	Push STORE CH, listen for mechanical tuning sound.	4.499.93.-
42	Push CALL, listen for relay click, observe Power Format reverting to Normal Display Format after 2 seconds.	
43	Push '1', observe 100 Hz increment displayed.	:.13.
44	Push '+', observe frequency increases by 100 Hz on that displayed at Step 41.	4.500.0:-.-
45	Push CANCEL	4.500.03.-
46	Enter 7.999.9	7.999.93.
47	Push STORE CH, listen for mechanical tuning.	7.999.93.-
48	Push CALL, listen for relay click, observe Power format reverting to Normal Display format after 2 seconds.	
49	Push '1', observe 100 Hz increment displayed.	:.13.
50	Push '+', observe frequency increment by 100 Hz on that displayed at Step 46.	8.000.0:-.-
51	Push CANCEL	8.000.03.-
52	Enter 14.999.9	14.999.93.
53	Push STORE CH, listen for mechanical tuning	14.999.93.-

Table 2.3.3 First Line Functional Check - Keyboard Routine (Cont.)

STEP	PROCEDURE	REQUIRED INDICATION
54	Push CALL, listen for relay click, observe Power Format reverting to Normal Display Format after 2 seconds.	
55	Push '1', observe 100 Hz increment displayed.	. .1:3.
56	Push '+', observe frequency increment by 100 Hz on that displayed at Step 52.	15.000:-.-
57	Push CANCEL	15.000:3.-
58	Enter 30.000.0	30.000:3.-
59	Push STORE CH, listen for mechanical tuning.	30.000:3.-
60	Push CALL, listen for relay click, observe Power Format reverting to Normal Display Format after 2 seconds.	
	Test 11	
61	Push REC CH	30.000:3.
62	Push '1', observe right hand digit is 1.	XX.XXX:X.1
63	Push REC CH	XX.XXX:X.
64	Push '2', observe right hand digit is 2.	XX.XXX:X.2
65	Repeat for 3 to 9 and for 0. Observe correct channel number is displayed as right hand digit.	
	Note: If 4 MHz, Mode 1 display appears for any Channel this indicates that the Channel data may have been erased from memory. This erasure could result from keyboard operation or from a fault.	4.000:1.X
	Test 12	
66	At transceiver set rotary switch to K/B & ILL, check display illuminates for 10 seconds.	Display illuminated
67	Push any key, check display illuminates for 10 seconds.	Display illuminated
68	Set rotary switch to REM CON, observe display.	-.-IL.L:-.- Illegal Format
69	Set rotary switch to K/B & ILL.	
70	Push CANCEL.	Display illuminated for 10 seconds
71	Set rotary switch to REM CON, observe display.	Illegal Format

Table 2.3.3 First Line Functional Check - Keyboard Routine (Cont.)

STEP	PROCEDURE	REQUIRED INDICATION
72	Set rotary switch to K/B.	Normal Display Format
	Test 13	
73	Enter Test data as in Test 4.	1 7.4 5 0.0 3.-
74	Using 20 cm length of 20 SWG tinned copper wire connect AUDIO 1 socket, pin F to inner conductor of RT connector. Observe Option Format reverting to Normal Display Format after 2 seconds. Note: If first left hand digit of option format shows 1, then after option display AP will appear for 2 secs before reverting to normal display format.	Option Format Reverts to Normal Display Format
75	Push PWR	-.-.P 2 0. :-.0
76	Push '+'	-.-.P 1 0.0 :-.0
77	Push '-' twice	-.-.P 4 . :-.0
78	Push CANCEL	1 7.4 5 0.0 3.-
79	Remove link applied in Step 74. Observe Option Format reverting to Normal Display format after 2 seconds.	
80	Connect link between AUDIO 2 socket, pin F and inner conductor of RT connector. Observe Option Format reverting to Normal Display Format after 2 seconds.	
81	Push PWR	-.-.P 4 . :-.0
82	Push '+' twice	-.-.P 1 0.0 :-.0
83	Remove link applied in Step 80. Observe Option Format reverting to Normal Display Format after 2 seconds.	
84	Push PWR	-.-.P 2 0. :-.0
85	Push '-'	-.-.P 4 . :-.0
	Test 14	
86	Connect link between AUDIO 1 socket pins F and B listen for relay click and observe display.	1.-.P 4 . :-.1
87	Remove link applied in Step 86, listen for relay click and observe display.	-.-.P 4 . :-.0
88	Push '+'	-.-.P 2 0. :-.0

Table 2.3.3 First Line Functional Check - Keyboard Routine (Cont.)

STEP	PROCEDURE	REQUIRED INDICATION
89	Reconnect link between Audio 1 socket pins F and B, listen for relay click and observe display. Note: If transceiver battery is used, carry out following test: Connect a second shorting link from pin C to pin B of external supply connector (at rear of transceiver). Note display. Power output goes to low power, but indication remains at P20.	3 - . P 2 0 . : - . 3 1 - . P 2 0 . : - . 1
90	Disconnect link applied in Step 89 listen for relay click and observe display. Disconnect link from external supply connection.	- - . P 2 0 . : - . 0
91	Push '-'	- - . P 4 . : - . -
92	Set function switch to H/S. Reconnect link between Audio 1 socket pins F and B, listen for relay click and observe display.	1 - . P 4 . : - . 1
93	Remove link applied in Step 92, listen for relay click and observe display.	- - . P 4 . : - . 0
94	Set function switch to K/B.	
	Test 15	1 7 . 4 5 0 . 0 : 3 . 1
95	Push PWR	- - . P 4 . : - . 0
96	Repeat Test 14 with link applied now to Audio 2 socket pins F and B	As Test 15
	Test 16	
97	Set function switch to H/S	1 7 . 4 5 0 . 0 : 3 . -
98	Connect link between AUDIO 1 socket pins G and E.	Display blank
99	Remove link applied in Step 98.	Option Format Reverts to Normal Display Format
	Test 17	
100	Connect link between Audio 2 socket pins G and E, listen for relay click and observe display.	1 - . P 4 . : - . 1
101	Set function switch to OFF and remove link applied in Step 100.	Display blank

Table 2.3.4 First Line Performance Check - Receive Routine

STEP	PROCEDURE	REQUIRED INDICATION
1	Check Test Set TS 2010 in accordance with para. 8 of this Chapter.	
2	Set transceiver RT 2000 function switch to OFF. Connect Handset/Control Box to AUDIO 2 socket.	
3	Connect cable CX2014 between TS 2010 CALLPAC socket and the transceiver AUDIO 1 socket.	
4	Remove protective cover from cable CX2011.	
5	Remove 5 A fuse from transceiver, store in CX2011 protective cover.	
6	Connect cable CX2011 between TS 2010 and transceiver fuse holder.	
7	Connect cable CX 2010 between TS 2010 RX(LL) socket and transceiver RT connector.	
	Test 1 : Battery	
8	On TS 2010 set FUNCTION switch to Position A, hold down ON switch and monitor LED indication.	TS 2010 'ON' LED glows
9	Set transceiver function switch to K/B.	TS 2010 LED indication 14 or 15
	Notes: (a) Illumination of 14 and 15 is acceptable. (b) If any other indicator illuminates investigate transceiver battery.	
10	Release ON switch.	
	Test 2 : Rx Current	
11	Set TS 2010 set FUNCTION switch to Position F, hold down ON switch and monitor LED indication.	3 or 4
12	Set transceiver function switch to K/B & ILL.	5, 6 or 7
	Note: If indicator 3 illuminates in Step 11, 5 or 6 should illuminate in Step 12. If indicator 4 illuminates in Step 11, 6 or 7 should illuminate in Step 12.	
13	Release ON switch.	
14	Set transceiver function switch to K/B.	
15	Set TS 2010 FUNCTION switch to A.	
	Test 3 : Data Entry and Display	
16	At transceiver enter following data:	

Frequency	Mode	Channel
18750	8	1
25000	8	2
37500	8	3
56250	8	4
93750	8	5
131250	8	6
162500	8	7
256250	8	8
293750	8	9

Note: If for security reasons programming is not possible, each frequency is to be entered separately, as required, in the working Channel, go to step 20.

Table 2.3.4 First Line Performance Check - Receive Routine (Cont.)

STEP	PROCEDURE	REQUIRED INDICATION
17	If data has been entered, push REC CH.	
18	Push '1'	TRANSCEIVER DISPLAY 1.87 5.0 8.1
19	Push in turn, 2 to 9 inclusive, observe correspondence of display with stored Channel data.	
	Test 4 : Signal to Noise (Low Level)	
20	Set TS 2010 FUNCTION switch to B, hold down ON switch throughout steps 21 to 24 and monitor indications.	PHONE 1000 Hz Tone TS 2010 LED INDICATION 12, 13, 14 or 15
21	On transceiver, push '-', maintain key depressed.	PHONE 1000 Hz Volume decreases TS 2010 LED INDICATION 1 or 2
22	Push '+', maintain key depressed until indicator 14 glows.	PHONE 1000 Hz Volume increases TS 2010 LED INDICATION 14
23	Set TS 2010 FUNCTION switch to C.	PHONE Noise TS 2010 LED INDICATION 2, 3 or 4
24	Set TS 2010 FUNCTION switch to B.	PHONE 1000 Hz Tone
25	Push REC CH	
26	Push '2', listen for noise of band changing, observe indications. Note: If channels are not stored, enter second frequency into working channel.	TRANSCEIVER DISPLAY 2.50 0.0 8.2 TS 2010 LED INDICATION 12, 13, 14 or 15 PHONE Noise TS 2010 LED INDICATION 2, 3 or 4 PHONE 1000 Hz Tone
27	Repeat Steps 20 to 26 for Channels 3 to 9.	
	Test 5 : AGC and In Band Spurious Rejection	
28	Set TS 2010 FUNCTION switch to B.	
29	Transfer cable CX 2010 from RX(LL) to RX(HL) TX socket on TS 2010.	
30	On transceiver, enter 50000, mode 8.	TRANSCEIVER DISPLAY
31	Push STORE CH.	5.00 0.0 8.-

Table 2.3.4 First Line Performance Check - Receive Routine (Cont.)

STEP	PROCEDURE	REQUIRED INDICATION
32	At TS 2010 hold down ON switch and monitor indications.	PHONE 1000 Hz TONE TS 2010 LED INDICATION 14
33	If necessary push '+' for indicator 14 to light.	
34	Set TS 2010 FUNCTION switch to D, check tone still audible, LED 8 to LED 15 extinguished.	
35	Release TS 2010 ON switch.	
	Test 6 : Tune ATU	
36	At transceiver connect Dummy Antenna to front panel antenna mounting base, transfer cable CX 2010 from RT connector to Dummy Antenna and connect 'U' link across RT and ATU connectors.	
37	Set TS 2010 FUNCTION switch to B and hold down ON switch.	
38	Push TUNE	- - . - - - . - - : - . X
39	Push '+' and hold depressed.	
40	Push '-' and hold depressed.	Minimum value of X: 0, 1 or 2
41	Note that X goes to a minimum.	
42	Release TS 2010 ON switch.	
	Test 7 : Rx & ATU Current	
43	Set TS 2010 FUNCTION switch to F, hold down ON switch and monitor indications.	TS 2010 INDICATION 3 or 4
44	Push '+' or '-'	5, 6 or 7
45	Release TS 2010 ON switch.	
46	At transceiver remove 'U' link, transfer cable CX 2010 to RT connector.	
47	Remove Dummy Antenna.	
48	At TS 2010 transfer cable CX 2010 from RX(HL) TX socket to RX(LL) socket and set FUNCTION to B.	
	Test 8(a) : S/N For USB (Modes 6 and 9)	
49	At transceiver enter 24990, mode 6, push STORE CH.	
	Note: If CCIR option fitted enter 25010, mode 6.	
50	At TS 2010 hold down ON switch and monitor indications.	PHONE 1000 Hz Tone TS 2000 LED INDICATIOM 12, 13, 14 or 15
51	Set TS 2010 FUNCTION switch to C.	PHONE Noise TS 2000 LED INDICATION 2, 3 or 4
52	Set TS 2010 FUNCTION switch to B.	PHONE 1000 Hz Tone
53	Release ON switch	
54	Repeat Step 49 to Step 53 for mode 9.	

Table 2.3.4 First Line Performance Check - Receive Routine (Cont.)

STEP	PROCEDURE	REQUIRED INDICATION
	Test 8(b) : S/N For LSB (Modes 7 and 0)	
55	At transceiver enter 25010, mode 7, push STORE CH.	
	Note: If CCIR option fitted enter 24990, mode 7.	
56	Repeat Step 50 to 53.	
57	Repeat Step 55 and 56 for mode 0.	
	Test 9 : Frequency and Data Entry Checks	
58	At transceiver enter 175000, mode 8, push STORE CH.	
59	At TS 2010 hold down ON switch and monitor indications.	PHONE 1000 Hz Tone TS 2010 LED INDICATION 12, 13, 14 or 15 TRANSCEIVER DISPLAY 1 7.5 0 0.0 8. -
60	At transceiver push '1'	
61	Push '-' eight times.	PHONE Tone increases in pitch, silenced at eighth push. TS 2010 LED INDICATION 2, 3 or 4 TRANSCEIVER DISPLAY 1 7.4 9 9.2 - . -
62	Push '-'	PHONE Audio Tone
63	Repeat operation of '-' key. Audio tone increase in pitch until tone is silenced; Note display.	TRANSCEIVER DISPLAY 1 7.4 9 7.8 - . - or less
64	Push '+' repeatedly noting 100 Hz increments on display and decrease in pitch of tone. Note display when tone silenced. (Null point).	1 7.4 9 9.2 - . -
65	Repeat operation of '+' key to achieve display.	1 7.5 0 0.0 - . -
66	At TS 2010 release ON switch.	
67	Enter 187500, mode 8, push STORE CH, note display.	1 8.7 5 0.0 8. -
68	Repeat Step 59 to Step 61. Note display when tone silenced. (Null point).	1 8.7 4 9.2 - . -
69	Push CANCEL	
70	Enter 218750, mode 8, push STORE CH, note display.	2 1.8 7 5.0 8. -
71	Repeat Step 59 to Step 61. Note display when tone silenced. (Null point).	2 1.8 7 4.2 - . -
72	At transceiver push CANCEL, set rotary switch to OFF.	

Table 2.3.5 First Line Performance Check - Transmitter Routine

STEP	PROCEDURE	REQUIRED INDICATION
1	Carry out preliminary procedures in accordance with Step 1 to Step 6 of Receiver Routine (Table 2.3.4).	
2	Connect Cable CX 2010 between RX(HL)/TX socket on TS 2010 and transceiver RT connector.	
3	Set transceiver function switch to K/B	
4	Set TS 2010 FUNCTION switch to Position E.	
	Test 1 : Data Entry and Display	
5	Repeat Step 16 to Step 19 of Receiver Routine (Table 2.3.4) entering mode 3 for all Channels, observe display.	1.8 7 5.0 3.1
	Note: If using working Channel method, channel number is not displayed.	1.8 7 5.0 3.-
	Test 2 : Low Power and Battery Current (Mode 3)	
6	Confirm Steps 3 and 4 of this Routine.	
7	At transceiver push PWR, push '-', observe display.	- -.P 4 . :-.0
8	Operate pressel, observe indications.	PHONE 1000 Hz tone TRANSCEIVER DISPLAY 0 -.P 4 . :-.3
9	At TS 2010 hold down ON switch and monitor indications.	TS 2010 LED INDICATION 3, 4, 5 or 6
10	Release ON switch.	
11	Release pressel.	
12	Set TS 2010 FUNCTION switch to G.	
13	Operate pressel, listen for tone.	PHONE 1000 Hz tone
14	At TS 2010 hold down ON switch and monitor indications.	1000 Hz tone TS 2010 LED INDICATION 1, 2 or 3
15	Release ON switch.	
16	Release pressel.	
17	Set TS 2010 FUNCTION switch to E.	
	Test 3 : High Power and Battery Current (Mode 3)	
18	At transceiver push '+' and note display.	- -.P 2 0. :-.0
19	Operate pressel, observe indication.	PHONE 1000 Hz tone TRANSCEIVER DISPLAY 0 -.P 2 0. :-.7* or 8

Table 2.3.5 First Line Performance Check - Transmitter Routine (Cont.)

STEP	PROCEDURE	REQUIRED INDICATION
20	At TS 2010 operate ON switch and monitor indications.	TS 2010 LED INDICATION 11, 12, 13 or 14
21	Release pressel.	
22	Set TS 2010 FUNCTION switch to G.	
23	Operate pressel, listen for tone.	PHONE 1000 Hz tone
24	At TS 2010 hold down ON switch and monitor indications.	TS 2010 LED INDICATION 7, 8, 9, 10 or 11
25	Release ON switch.	
26	Release pressel	
	Test 4 : Battery Check (High Power Mode 3)	
27	At TS 2010 set FUNCTION switch to A, hold down ON switch and monitor indications.	14 or 15
28	Operate pressel, observe indications.	13 or 14
29	Release ON switch.	
30	Release pressel.	
31	Set TS 2010 FUNCTION switch to E.	
32	At transceiver push CANCEL.	
	Test 5 : Power Output and Current Drain (Channels 2 and 9)	
33	Repeat Tests 2 and 3 for Channels 2 to 9. Note audible mechanical noise indicating tuning and band changing taking place as each channel is selected.	
34	Observe and record transceiver display.	TRANSCEIVER DISPLAY LOW POWER Y - . P 4 . : - . X X = 2 or 3 Y = 0 or 1 HIGH POWER Y - . P 2 0 . : - . X X = 6, 7 or 8 Y = 0, 1 or 2
	Test 6 : ATU Tuning	
35	At transceiver fit dummy antenna to antenna mounting base, transfer cable CX 2010 to the dummy antenna, connect 'U' link across the RT and ATU connectors.	
36	Enter 174500, push STORE CH, push CALL and observe noise of tuning accompanied by single tone, followed by two tone note.	PHONE single tone then two tone

Table 2.3.5 First Line Performance Check - Transmitter Routine (Cont.)

STEP	PROCEDURE	REQUIRED INDICATION
37	Operate pressel, observe indications.	Single tone TRANSCEIVER DISPLAY X - . P 2 0 . : - . Y X = 0, 1 or 2 Y = 6, 7 or 8
38	At TS 2010 confirm FUNCTION switch to E, hold down ON switch and monitor indications.	TS 2010 LED INDICATION 9, 10 or 11
39	Release ON switch.	
40	Release pressel.	
41	At transceiver remove 'U' link, transfer cable CX 2010 to RT connector, remove dummy antenna.	
	Test 7 : Power Output, Mode 1, 2, 4 & 5	TRANSCEIVER DISPLAY
42	At transceiver enter mode 1, push STORE CH and note display.	1 7 . 4 5 0 . 0 : 1 . -
43	At TS 2010 hold down ON switch.	
44	Operate pressel, count 1 to 10 with handset in normal operational position not too close to the mouth, monitor indications.	TS 2010 LED INDICATION 1 to 12 flicker
45	Retain pressel operation, observe display.	TRANSCEIVER DISPLAY 0 - . P 2 0 . : - . X X = 5, 6 or 7
46	Whistle into mouthpiece.	TS 2010 LED INDICATION 11, 12 or 13
47	Release ON switch.	
48	Release pressel.	
49	Repeat Step 42 to Step 48 for modes 2, 4 and 5. Results will be similar for mode 2. For mode 4 and 5 X in step 45 will be smaller for the same level of input and indicators from 6 to 13 will flicker during Step 46.	
50	Set transceiver rotary switch to OFF.	
51	Remove cable CX 2011 and replace 5 A fuse in transceiver.	
52	Replace CX 2011 protective cover.	
53	Remove and stow remaining cables.	

Table 2.3.6 Receiver/Transmitter RT 2000 Alarms

Alarm	Cause and Action
1 kHz tone burst repeated at 6 sec. intervals. Display showing BA at 6 sec. intervals.	Indicates low battery volts. Transceiver may still be used but battery must be replaced or recharged (as appropriate) as soon as possible
Continuous pulsating tone. Display showing PH at 6 sec. intervals.	Synthesiser not locked. Re-select channel or enter frequency again.
Continuous pulsating tone. No display message.	1 Transceiver protection against high incoming signal level. Check proximity of transmitter. 2 Rotary Switch set to STORE position.

Table 2.3.7 Receiver/Transmitter RT 2000 Fault Symptoms

Symptoms	Action
1 No noise in earpiece.	1 Check Rotary Switch is set to H/S, K/B or K/B & ILL. 2 Check that H/S volume is turned up (clockwise). 3 Check display; If blank, check 5 A fuse. 4 Press and hold '+' key for 10 seconds. 5 Check battery is charged (replace if necessary). 6 Check connections. 7 Check that the transmit pressel is not operated.
2 ATU does not tune.	1 Check selected mode, if modes 6, 7, 8, 9 or 0 are selected, auto tuning is inhibited. 2 Check transmit pressel operates. 3 Check connections. 4 Check tuning and matching adaptors are fitted.
3 No or poor communications	1 Check display shows correct frequency, mode and channel number. 2 Operate transmit pressel and speak into microphone; check that the display shows high forward and low reverse power indications. If not, check antenna and connections and re-tune antenna. 3 Check audio ancilliaries and connections.
4 Connections and indications appear correct but fault remains.	1 Check transceiver using First line and and Performance Checks. If a fault is diagnosed, return transceiver to field repair

Table 2.3.8 Handset/Control Box Routine Fault Diagnosis

Test	Action	Observation	Suspected fault and module affected
1	Rotary switch to H/S	No display	H/S volume switch 'off'. Battery/fuse/PSU.
		BA intermittently	Change battery.
		No tone - no noise	Handset.
		Tone - no noise	Signal path faulty in transceiver, change to new channel. Still faulty - change transceiver. (ATU/RF Head/Phasing module)
		Display not as expected	See Notes 1, 2 and 3.
2	Push + & keep depressed Push - & keep depressed	Audio output does not change	Change transceiver. (K/B or channeliser module)
3	Push CALL	Display not as predicted Audio tone not as expected	Change transceiver. (ATU/channeliser)
4	Pressel (Tx)	Display not as expected Audio tone not as expected	See Note 4. Change transceiver. (Phasing/RF Head/ATU/PA/channeliser)
5	Channel change	Display does not change No change No change 4000.0:1.	Change to other channels. Change H/S. Change transceiver. For all channels: memory cleared (return transceiver for reprogramming or repair). See Note 3.

Notes:

1 If BA appears at the left of the display, accompanied by a warning audio tone, at intervals of 3 to 5 seconds, or if there is no display, this is an indication that the battery is low and should be changed and recharged.

2 If PH appears on the display, this is an indication of phase-lock loss, and another channel should be tried. If the display still shows PH, change the transceiver.

3 If the display shows 4 MHz Mode 1 for all channels, this indicates that the memory has been intentionally cleared or that a loss of data has occurred in the channeliser module. Return transceiver for reprogramming or repair.

4 When CALL or pressel are initiated after switching on or changing channels, the tuning sequence will take place. This will be indicated by the display changing, and a continuous audio tone will be heard in the phone.

5 AP on display signifies Callpac is suitable for Amplifier operation. First digit of option format is 1.

Table 2.3.9 Keyboard Routine Fault Diagnosis

Test No	Function checked	Suspected fault or faulty module
1	Rotary switch-on	Battery/Fuse/PSU/Channeliser
2	PA-ATU Link	No volts at ATU inner coax connector Wiring at ATU coaxial termination
3 to 8	K/B data entry	K/B - Channeliser
9	K/B Tx capability	Channeliser/PA
10	K/B - frequency incrementing	Synthesiser/Channeliser/ATU
11	K/B - VCO band edges	Synthesiser/PA
12	K/B - channel recall	Channeliser
13	Rotary switch - ILL	Switch/Lights/Channeliser
14 to 18	Handset simulation	Wiring to Audio 1 & 2/Channeliser

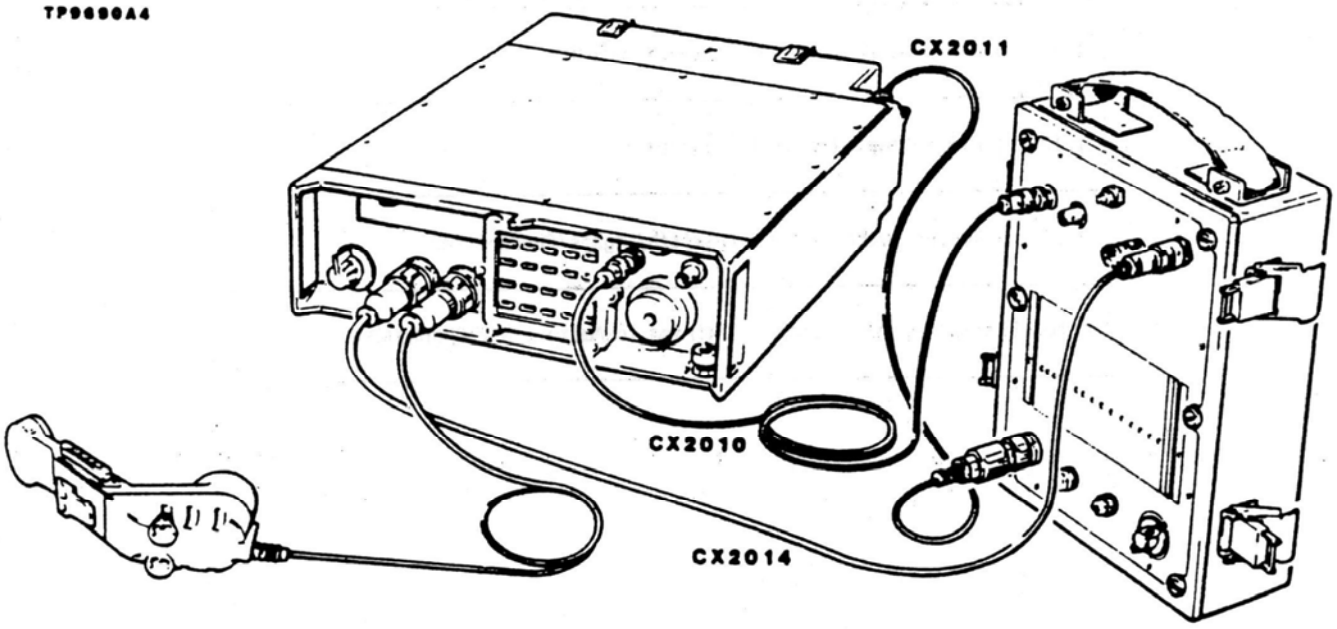


Fig 2.3.4 Typical Test Configuration

CATEGORY 3

TECHNICAL DESCRIPTION

Contents

CHAPTER 3.0

INTRODUCTION AND FUNCTIONAL DESCRIPTION

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Illustrations

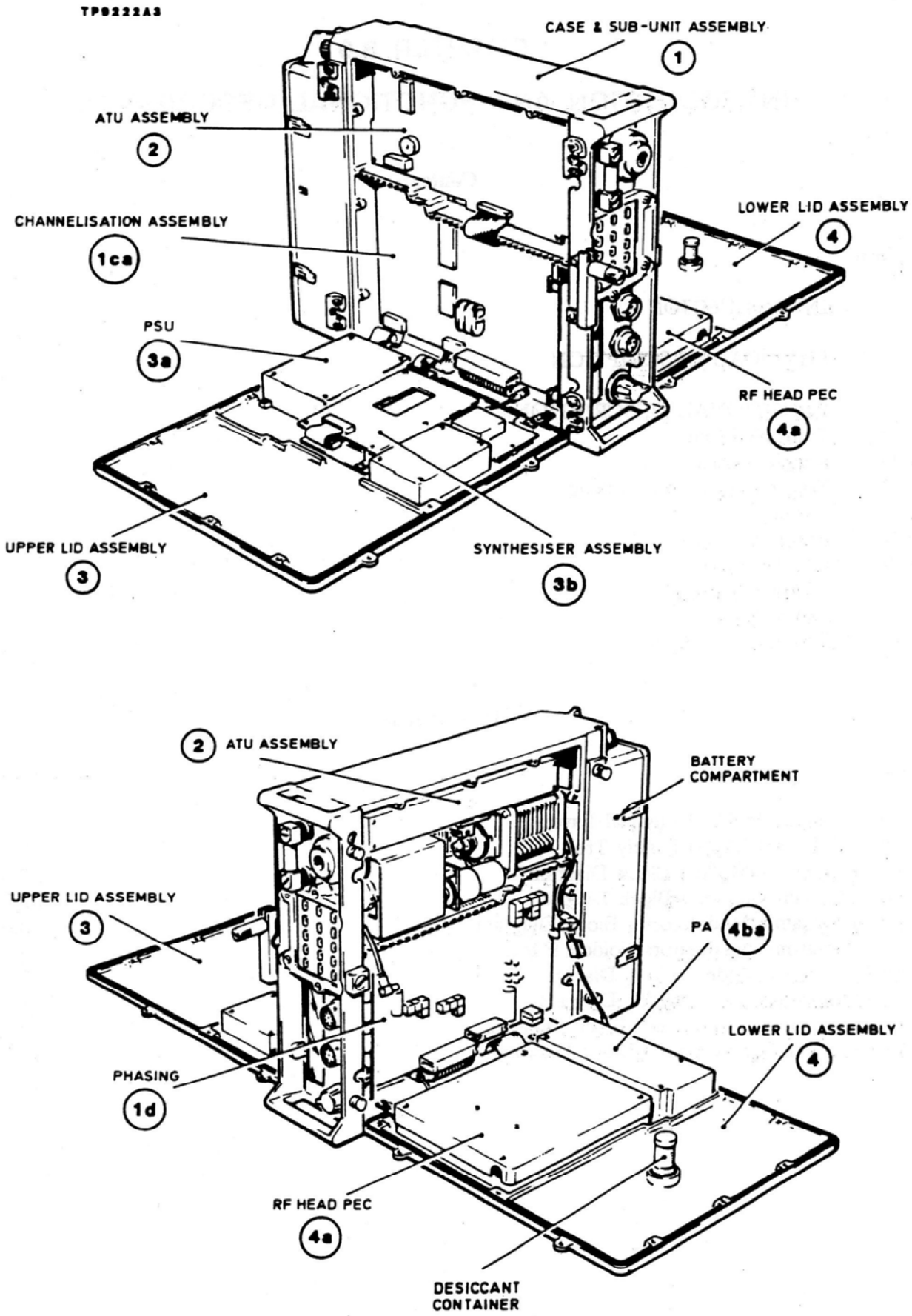


Fig 3.0.1 Callpac RT2000 Physical Layout

CHAPTER 3.0

INTRODUCTION AND FUNCTIONAL DESCRIPTION

INTRODUCTION

1 Callpac Transmitter/Receiver RT 2000 provides single side band (ssb) voice or data communication, or continuous wave (cw) morse communication on any one of 284,000 channels within the frequency band 1.6 to 30 MHz. Channel frequency and mode may be selected manually from the keypad, but for ease and speed of selection the frequency and mode data for up to ten channels can be preset in memory for immediate recall when required.

2 For voice transmission, a system of speech processing is used that effectively increases the mean transmitted power level. This facility is automatically switched in or out of circuit according to the selected operating mode.

3 The frequency spectrum covered by Callpac is divided into a number of bands each requiring a different set of filters. All bandswitching and tuning throughout the transceiver is fully automatic, so any frequency within the spectrum can be called for via the keypad. The microprocessor control system determines in which band the demanded frequency lies and selects the appropriate filters in the Antenna Tuning Unit (ATU).

PHYSICAL DESCRIPTION

4 The transceiver comprises three main parts, a central unit to which are hinged upper and lower panels (Fig 3.0.1). All three parts are aluminimum alloy castings, the outer plates having an 'O'-ring seal round the outer edge so that, when closed, the unit is impermeable to gas or water. Fig 3.0.1 shows the location of the various sub-assemblies and the circled numbers and letters refer to the Family Tree shown in Fig 3.0.2.

5 Interconnections between the sub-assemblies are provided by floating connectors and ribbon-strip cable. With the top and bottom panels opened, any PEC or sub-assembly can be easily removed for servicing or replacement without disturbing other sub-assemblies.

6 All band-switching (ie filter switching) and tuning takes place in the ATU, by means of a small dc motor and gearbox. Other filters in the system are fixed-audio frequency af filters.

FUNCTIONAL DESCRIPTION

Note: Reference to ICs in text are related to ML and/or U on circuit diagrams.

7 A general idea of the system can best be obtained by following the signal paths through the unit, first in the 'transmit' mode and then in the 'receive' mode.

Transmit Mode (Fig 3.0.3)

8 Microphone signals are first filtered and then fed to a buffer amplifier on the Phasing PEC. The output from the amplifier feeds two signal paths, sidetone and transmit. The sidetone signal is an audio representation of the input (speech or cw) and is fed to the audio sockets via a pair of voltage controlled amplifiers (volume control), while the transmit signal is regulated in the Voice Operated Gain Adjusting Device (VOGAD). Noise reduction is achieved by passing

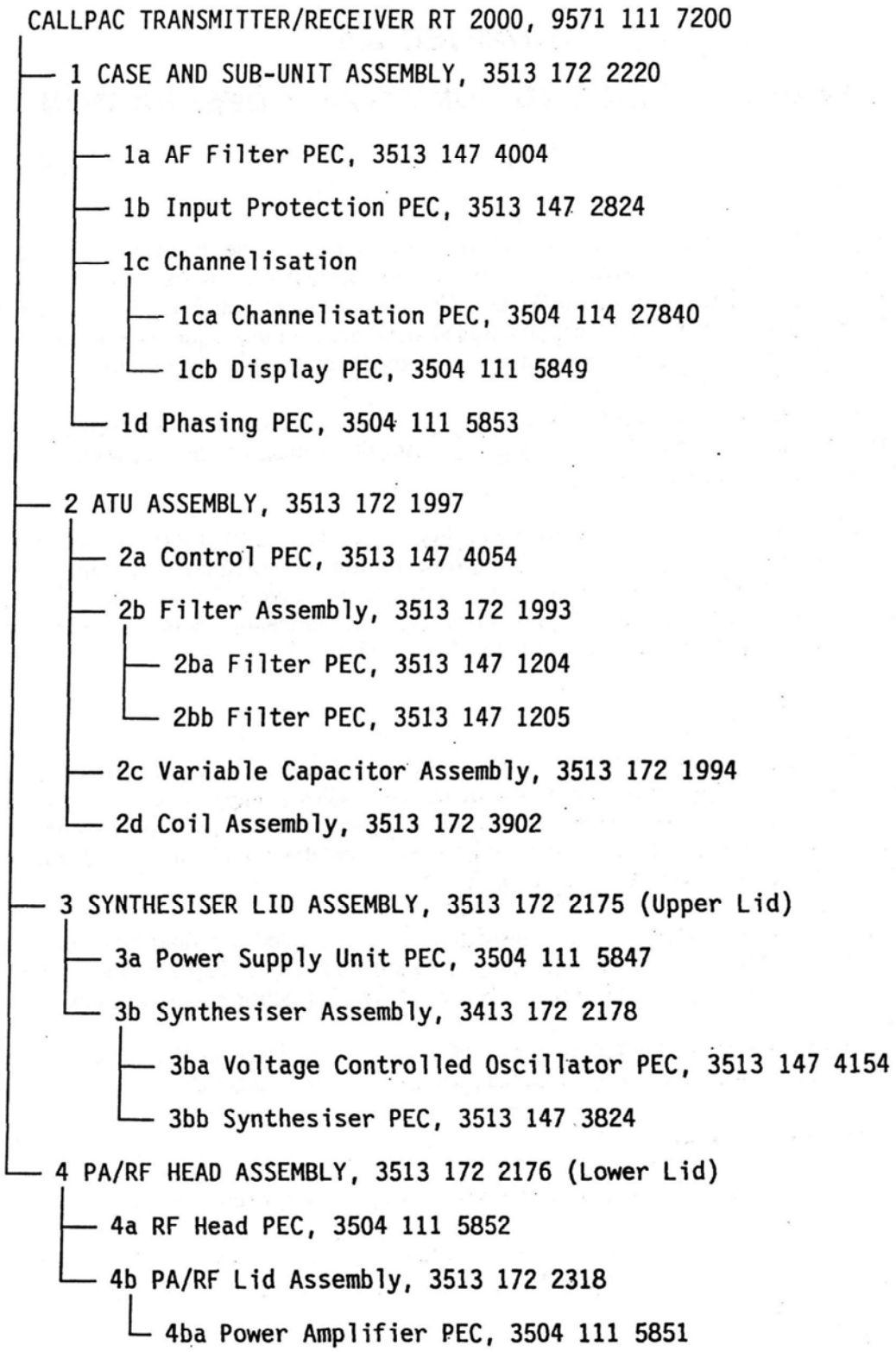


Fig 3.0.2 Callpac RT2000 Family Tree

the signals through a 0.3 kHz to 3.3 kHz bandpass filter, after which they are divided into two components identical in amplitude and frequency but with a 90° difference in phase (phase quadrature related). The two outputs are then fed to two balanced modulators within the speech clipper circuit (Fig 3.0.4).

9 Each modulator is driven by a different output from a divide-by-four frequency divider. A 1.024 MHz signal from the Synthesiser PEC is applied to the divider to produce two 256 kHz carrier signals with 90° phase difference. These signals are selected so that the 0° af signal is combined with a 90° carrier signal, while the 90° af signal is combined with a 0° carrier signal. The outputs from the modulators consist of both upper and lower sidebands. The phase relationship of these outputs is such that, because the positive output of one modulator is connected to the negative output of the other, the upper sidebands are subtractive and cancel each other out while the lower sidebands are additive to produce the required ssb signal. A bandpass filter removes any unwanted modulator frequency components.

10 To increase the average power transmitted, the high peaks produced by the human voice must be reduced. This is achieved by passing the ssb signal through a clipper circuit. Any unwanted harmonics are filtered out by a further bandpass filter.

11 Conversion of the ssb signal back to audio frequency (af) signals is carried out by two further modulators each fed with the same 256 kHz reference supplied to the previous modulators. Two operational amplifiers act as low-pass filters on the output line, allowing only the 0° and 90° elements to pass onto the balanced modulator circuit. Speech clipping is bypassed when Data Transmission Mode is in use (para 19).

12 Paras 12 to 15 describe the balanced modulator circuit with lsb (lower sideband). Para 16 covers changes to that description resulting from usb (upper sideband) selection. The two audio outputs from the speech clipper circuit are applied to two balanced modulators (M1 and M2) as shown in Fig 3.0.5. Each modulator is also supplied with an audio tone (fo) of 1.8 kHz which is 90° out-of-phase with its audio input (f). The modulators are balanced so as to remove both the audio tone and the audio input and leave only the sidebands (f_0-f) and (f_0+f). In this case the lower sideband is selected and is 'folded', that is to say that it contains all the original information in a bandwidth of half the audio input.

13 This 'folded' effect is achieved by correct selection of the audio tone (fo) so that it is centred on the bandwidth set by the 0.3 to 3.3 kHz bandpass filter (ie 1.8 kHz). For audio input frequencies (f) of 0.3 to 1.8 kHz the lower sideband (f_0-f) will be 1.5 kHz down to zero (Fig 3.0.6a). Audio input frequencies (f) of 1.8 to 3.3 kHz produce beat frequencies of zero up to 1.5 kHz (Fig 3.0.6b). The 'folded' effect occurs whenever both the above states occur together (Fig 3.0.6c).

14 The phase relationship of the sidebands produced by modulators M1 and M2 (Fig 3.0.5) is such that, because the positive output of M2 is combined with the negative output of M1, the upper sideband is cancelled out and the lower sideband is reinforced and fed to the RF Head as CH2TX.

15 An identical circuit (M3 and M4) receives the same two audio inputs (f), and an audio tone of 1.8 kHz which this time is in phase with f. The positive output of M3 is combined, via Combiner A2 with the positive output of M4 so that the upper sideband is again cancelled out.

16 With usb selected, the microprocessor on Channelisation produces a usb selection signal. This signal, when passed through the usb/lsb logic circuit (Fig 3.0.5) provides the programming information required by the divide-by-four stage to change the phase of the f_0 signal applied to modulators M1 to M4. This changes the phase relationship of the sidebands produced by the modulators such that when they are combined in A1 and A2 the lower sideband is cancelled out and the upper sideband is reinforced and fed to the RF Head as CH1TX and CH2TX (a 90° phase difference exists between the two).

17 In the RF Head the two signals are once more filtered (the principal purpose of the successive filter stages is to remove spurious higher frequency components, eg unwanted sidebands and noise). The selected transmission frequency, derived from a voltage controlled oscillator (VCO) in the Synthesiser, is also fed to the RF Head where it is subjected to phase-changing to produce two signals in quadrature. These, together with the af signals, are applied to two final balanced modulators whose outputs, after combining, produce the required ssb rf signal. The suppressed residual unwanted sideband lies in the same frequency band as the wanted signal and so cannot cause adjacent channel interference. The rf signal is passed through an amplifier whose gain is controlled by Automatic Level Control (ALC); this is simply a circuit that ensures a constant radiated signal regardless of variations in power supply level, operating temperature or voltage standing wave ratio (VSWR).

18 The rf signal passes through a bandpass filter, located in the ATU, which will have been selected automatically when the transmission frequency was chosen, and then into the Power Amplifier (PA). The gain of the PA is determined by a bias control circuit that can be set to either of two conditions as determined by the choice of high or low power transmission. Further control of the PA is governed by the amplifier protect circuit, which contains ALC, a temperature sensor and a VSWR detector (high temperature or poor VSWR lowers the gain of the PA).

19 For data transmission the speech clipper circuit is bypassed and the quadrature af signals at input frequency (para 8) are applied directly to the balanced moduators (para 11). Switching signals are derived from Channelisation. In the case of cw operation (Morse) a keying input is applied to the CH2TX input in the RF Head. This keying input switches on the CH2TX balanced modulator to transfer rf, at the selected channel frequency, to the output stages in the same way as an ssb signal.

Receive Mode (Fig 3.0.7)

20 Many of the transceiver sub-assemblies are common to both transmit and receive modes. After filtering in the ATU, the received signal passes to the RF Head where it is amplified in an automatic gain controlled (AGC) amplifier. A phase splitter divides the signal into two components, which are then applied to two balanced modulators. These are driven by quadrature demodulating signals at the channel frequency. The outputs from this demodulating stage are 'fold-over' side bands of the required audio base band signal. After filtering and amplifying in low-noise af amplifiers, the signals are fed to Phasing as CH1RX and CH2RX.

21 After further AGC controlled amplification, CH1RX and CH2RX are again applied to balanced modulators for the final demodulation. The output from one of the channels is also used as the input signal for the AGC generator. Demodulation is achieved by mixing CH1RX and CH2RX audio base band signals with two quadrature signals at 1.8 kHz. The resulting outputs from two balanced modulators are combined in an audio amplifier, to produce the wanted demodulated sideband signal; the unwanted sideband signal is suppressed. The usb or lsb is selected by switching the phase of the 1.8 kHz signals as on transmit. The audio signal is then

filtered and further amplified in a stage to which volume control is applied. The signals are then fed via AUDIO 1 and AUDIO 2 outputs to the handset or headset.

22 The final stages of filtering and audio amplification can be used if required as an intercom channel between two operators. This facility may be selected from a handset or keyboard and does not interfere with normal radio reception.

Transmit/Receive Switching

23 Control signals from Channelisation determine the transceiver condition. Most of the switching is performed by changing the bias level on the appropriate amplifiers to turn them on or off, but relay switching is also used in the ATU. In transmit/receive mode, receive circuits are switched off before the transmit circuits are switched on. Conversely, the transmit circuits are switched off before the receive circuits are switched on. For receive only modes, the transmit circuits are permanently inhibited and the receive circuits permanently enabled. A set of inverting buffer amplifiers prevents interconnection of switched items through the control lines. A control line, TX/RX 3, is used to route a sidetone to the audio sockets.

Standby

24 This facility is available only via the Audio 1 output socket, and it allows an operator using a handset connected to that socket to switch the equipment to Standby by rotating the volume ON/OFF control fully anti-clockwise.

CAUTION: The facility is not available via the Audio 2 socket.

Antenna Tuning

25 The antenna is tuned and matched to the transceiver by the ATU automatically or manually (via the keypad). For tuning purposes, the frequency spectrum of 1.6 to 30 MHz covered by the transceiver is divided into nine frequency bands. According to the frequency of the channel selected, eight bandpass filters throughout the transceiver and the coarse tuning components in the ATU are switched automatically by an electric motor drive. Fine tuning of the ATU is driven by a second motor, controlled by a signal from the VSWR detector for automatic tuning or by keyboard inputs for manual tuning.

26 In a transmit mode, rf energy from the PA is applied to a switchable auto-transformer via the VSWR detector. The antenna tuning circuit consists of a switchable inductor in parallel with a variable capacitor. The auto-transformer provides impedance matching between the parallel tuned circuit and the PA. On channel change, signals from Channelisation and operation of a position sensing switch, cause the band select motor to drive the auto-transformer and inductor to the appropriate tappings. A series loading coil, limiting the peak voltage across the variable capacitor, is introduced when the lowest frequency band is in use.

27 Coincident with coarse tuning, signals from Channelisation normally cause the fine tune motor to run the variable capacitor to an end stop position of minimum capacitance. The channelisation signals then initiate a brief cw transmission during which the output from the VSWR detector runs the fine tune motor to the tuning position that gives minimum VSWR.

28 On changing channel in a receive only mode, coarse tuning takes place as previously described but, for operation under conditions of radio silence, fine tuning is transferred from VSWR detector control to operator control. This is done by selecting TUNE and operating the '+' or '-' keys on the keyboard. The operator tunes for maximum received signal strength indication on the Liquid Crystal Display or for best receiver performance.

Channelisation (Fig 3.0.8)

29 A microprocessor, linked by an address/data bus to input and output buffers, an analogue-to-digital converter and memory, enables Channelisation to accept control inputs from the operator, store information and extend control in digital format to the transceiver circuits.

30 When the transceiver is switched on by operation of the rotary switch on the front panel, power is applied to the Synthesiser and to Channelisation. After a delay for circuits to stabilize, the micro-processor begins to run the main program, stored in read only memory (ROM), using preselected channel information stored in random access memory (RAM).

31 Communication between the microprocessor and associated circuits is maintained through the address/data bus, controlled by timing and status signals generated within the microprocessor from 1.024 MHz clock pulses supplied by the Synthesiser. The contents of the RAM can be altered using the keyboard. An optional storage protection circuit safeguards the information and will allow alteration if a BA1233 Programme Store Key is inserted in the transceiver Audio 2 socket. Operator requirements are entered using the front panel rotary switch, keyboard, handset or control box and are processed in Channelisation for storage in RAM. ROM is non-volatile and therefore unaffected by switching off the transceiver, however, RAM requires a backup circuit to prevent loss of operator requirements. It consists of an auxiliary battery and a control circuit maintaining a trickle charge from the transceiver battery or from an external supply. Retention of information stored in RAM is ensured for up to 12 months by this safeguard.

Note: If lithium batteries are fitted, the trickle charge is not maintained.

Frequency Synthesis (Fig 3.0.9)

32 In both transmit and receive modes (Fig 3.0.3 and 3.0.7 respectively) a signal at four times the demanded frequency is required by the RF Head in order to produce two signals at the demanded frequency, but with a 90° phase difference. The required signal is derived from a pair of VCOs, one covering the frequency range 12.8 to 36 MHz and the other covering 60 to 120 MHz. Either VCO output can be used direct or via a divide-by-two circuit. Thus the overall range is 6.4 to 120 MHz in four bands. Band selection is determined by bits 1 and 2 of the 24-bit data input word from Channelisation. The remaining bits represent the demanded frequency in steps of 100 Hz. Bits 5 to 24 of the data word, taken as five groups of four bits, are binary coded decimal (BCD) representations of the digits in the demanded frequency, from 1s of MHz to 100s of Hz. Since only numerals 0, 1, 2 or 3 are needed to represent 10s of MHz, only two bits are required in the data word, these are bits 3 and 4.

33 The output frequency from the VCOs is determined by a frequency synthesiser integrated circuit (IC) and a variable ratio divider (universal divider). If the demanded frequency is an exact multiple of 1 kHz (ie 100 Hz digit is zero), the following description (para 34) applies. Otherwise (100 Hz digit non-zero) the operation of the universal divider IC is modified to include a side-stepping process (see para 36).

34 The serial data input word is stored in a shift register. Bits 3 to 20 are loaded into the universal divider (UD). The division ratio of the UD is obtained by means of a series of dividers whose modulus of division can be varied according to programming data applied to it. In practice, the division ratio n is set to a value such that a signal f^{out} whose frequency is four times the demanded frequency is divided to give a UD output frequency of 4 kHz. Because the UD has a maximum operating frequency of 15 MHz, whereas the VCO ranges up to 120 MHz, some pre-division is necessary before the VCO output can be applied to the UD. This division takes place in a pre-scaling divider. For the purpose of this description, the pre-scaling and UD functions can be regarded as a single function.

35 The frequency synthesiser IC contains a series of dividers, a phase modulator and two phase comparators (PC1 and PC2). A 5.12 MHz crystal oscillator provides the frequency standard for the transceiver. After division by 10, the crystal oscillator output is applied to the frequency synthesiser IC where it is further divided down to an output frequency of 4 kHz. This is the reference signal with which the UD output signal (f^{out}/n) is compared in the phase comparators. When (f^{out}/n) = 4 kHz the Synthesiser is in 'phase lock' and a signal indicating this is sent to Channelisation.

36 If the VCO output frequency is not four times the demanded frequency (ie f^{out}/n is not 4 kHz) the difference in frequency will produce an output voltage from the phase comparators. This is applied, via a loop filter, to the varicap diodes in the VCO; the sense of the voltage is such that the frequency of the VCO is driven in the direction required to approach the required frequency. The voltage on PC2 provides a coarse adjustment to drive the VCO until its output phase is within the control range of PC1, which then takes over the tuning with a fine adjustment. Another output from PC2 gives the indication of phase lock.

37 When the 100 Hz digit in the demanded frequency is other than zero the operation of the universal divider IC is modified. This is necesary because a demanded frequency that includes sub-multiples of 1 kHz (ie sub-multiples of 4 kHz at the VCO output) obviously requires a non-integral value of n to make f^{out}/n = 4 kHz. As it is not practical to make n a non-integer, it is arranged, instead, that the average value of n has the required non-integral value. This is done by increasing the division ratio to n + 1 for a certain proportion of comparison periods (a comparison period is ¼ ms). Bits 21 to 24 of the data input (ie the 100 Hz digit) are fed to a 'rate increase' circuit which produces a number of output pulses ($\overline{RI}$) equal to the decimal digit in the 100 Hz position, eg if the demanded frequency ends with 300 Hz then three $\overline{RI}$ pulses are generated in every ten comparison periods. These are applied to the $\overline{RI}$ input (rate increase) of the UD, causing it to increase its division ratio by 1 in three out of ten comparison periods. This is the 'side-stepping' process referred to in para 32.

38 Because the comparison periods now contain varying numbers of cycles, there is a phase jitter on the 4 kHz signal (OFS) from the UD. If this jitter were to reach the phase comparator it would produce a ripple on the output voltage, which would cause frequency modulation of the VCO output signal. The jitter is removed by the circuits represented in Fig 3.0.9 by the auto-null PEC, jitter predict and D-A converter, all of which contribute to the signal applied to the MOD input of the frequency synthesiser IC.

39 Bits 3 to 8 (10s and 1s of MHz) are fed to the auto-null circuit because the amplitude of the jitter varies according to the operating frequency; the amplitude of the correcting signal at MOD must therefore be similarly varied. Using only the tens and units of MHz gives sufficient accuracy for the purpose. The output of the auto-null circuit is a dc voltage that is constant if there are no 100s of Hz (bits 21-24 all zero) but otherwise depends on bits 3 - 8. This voltage

in turn is multiplied in the D-A converter by the output from the 'jitter predict' circuit. The resulting MOD signal therefore takes account of the 100s of Hz and also the position of the demanded frequency in the overall frequency spectrum of the system. V' is the signal actually compared with the 4 kHz reference; it is simply the input signal V with any phase jitter removed.

Power Supplies

40 The transceiver is powered internally by a 15 V nickel-cadmium rechargeable battery or externally from a 15 V supply. A 5 A fuse provides current protection in the supply to the Power Amplifier and Input Protection PEC. The Input Protection PEC provides protection against reverse polarity from an external power supply. It also provides current protection, using a 1 A fuse, in the unregulated voltage supply to the Power Supply Unit (PSU).

Power Supply Unit (Fig 3.0.10)

41 Power required by the transceiver components is produced in the PSU. A switched mode power supply circuit is used to provide the regulated voltage levels:

(a)	+12 V	:	Channelisation, ATU, and Phasing
(b)	+6 V (2 off)	:	Operational Amplifiers and Automatic Gain Control (AGC)
(c)	+5 V	:	Logic Circuits
(d)	-6 V	:	Operational Amplifiers

The +6 V for the Operational Amplifiers, +12 V, +5 V and -6 V supplies are referenced to case earth. The +6 V AGC supply is referenced to its own 0 V line.

42 Filtering of the unregulated dc supply to the PSU provides a smoothed supply for a series chopper and reduces any voltage transients. Switching of the chopper is synchronised with the switching of the dc-to-dc converter in the PSU; off switching being controlled by the voltage regulator. The mark-to-space ratio of the resultant square wave is adjustable, via the regulator, to maintain the direct voltage level from the flyback circuit at +5 V.

43 The dc-to-dc converter contains a free-running oscillator, operating at 20 kHz, supplied by the +5 V output of the flyback circuit. Transformation and rectification of the converter output produces direct voltage levels which, together with the +5 V from the flyback circuit, are filtered to provide the stabilized supplies for the transceiver components. Output short circuit protection is maintained by monitoring the flyback circuit current and adjusting the chopper mark-to-space ratio accordingly. Over-voltage protection is achieved for each stabilized output by voltage regulating diodes.

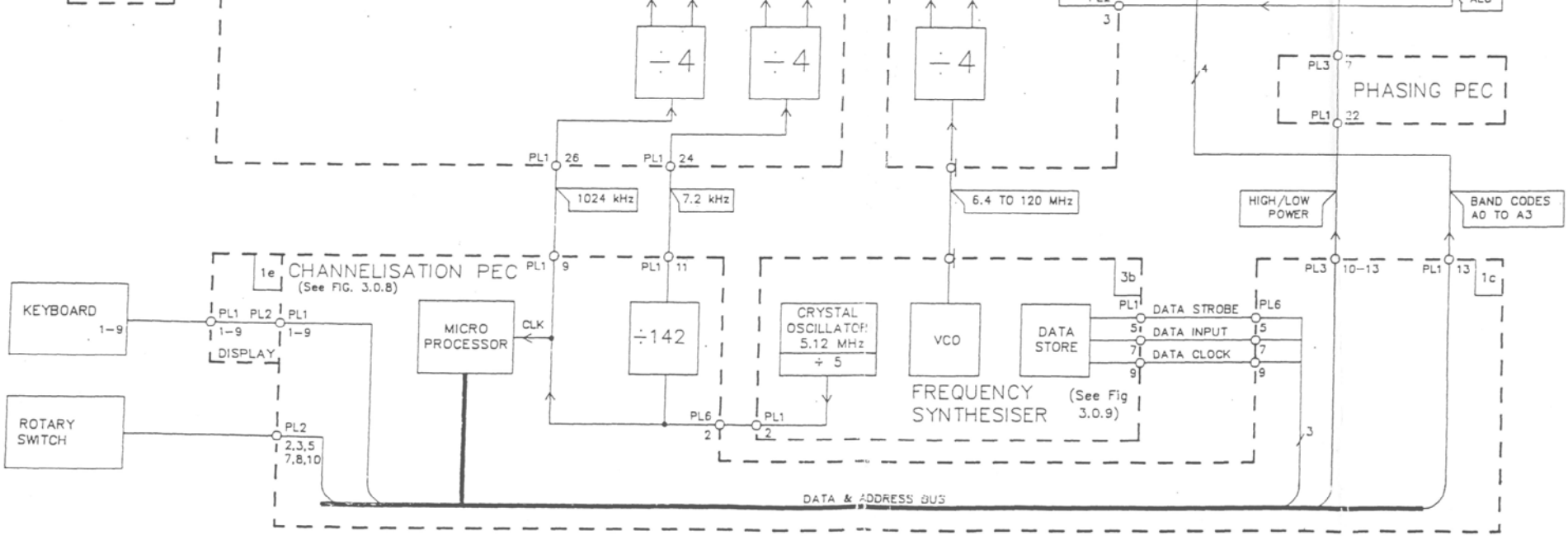
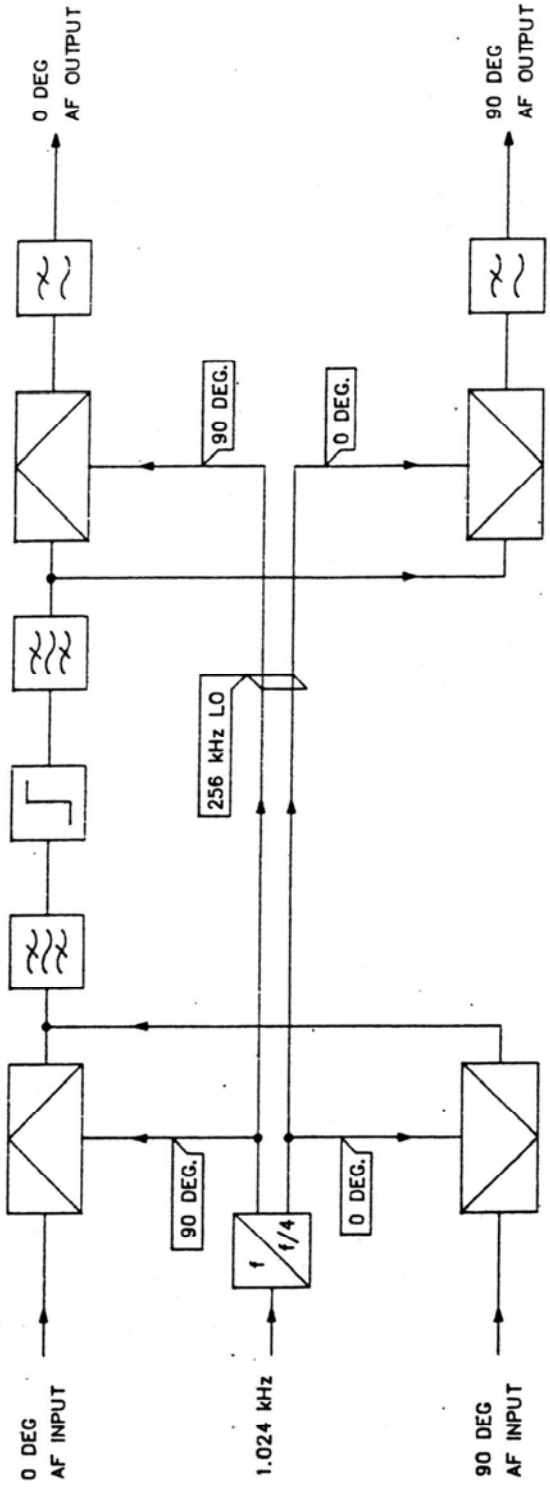


Fig 3.0.3

Transmit Mode : Block Diagram

Fig 3.0.3



IP9955C

Fig 3.0.4 Speech Clipper : Block Diagram

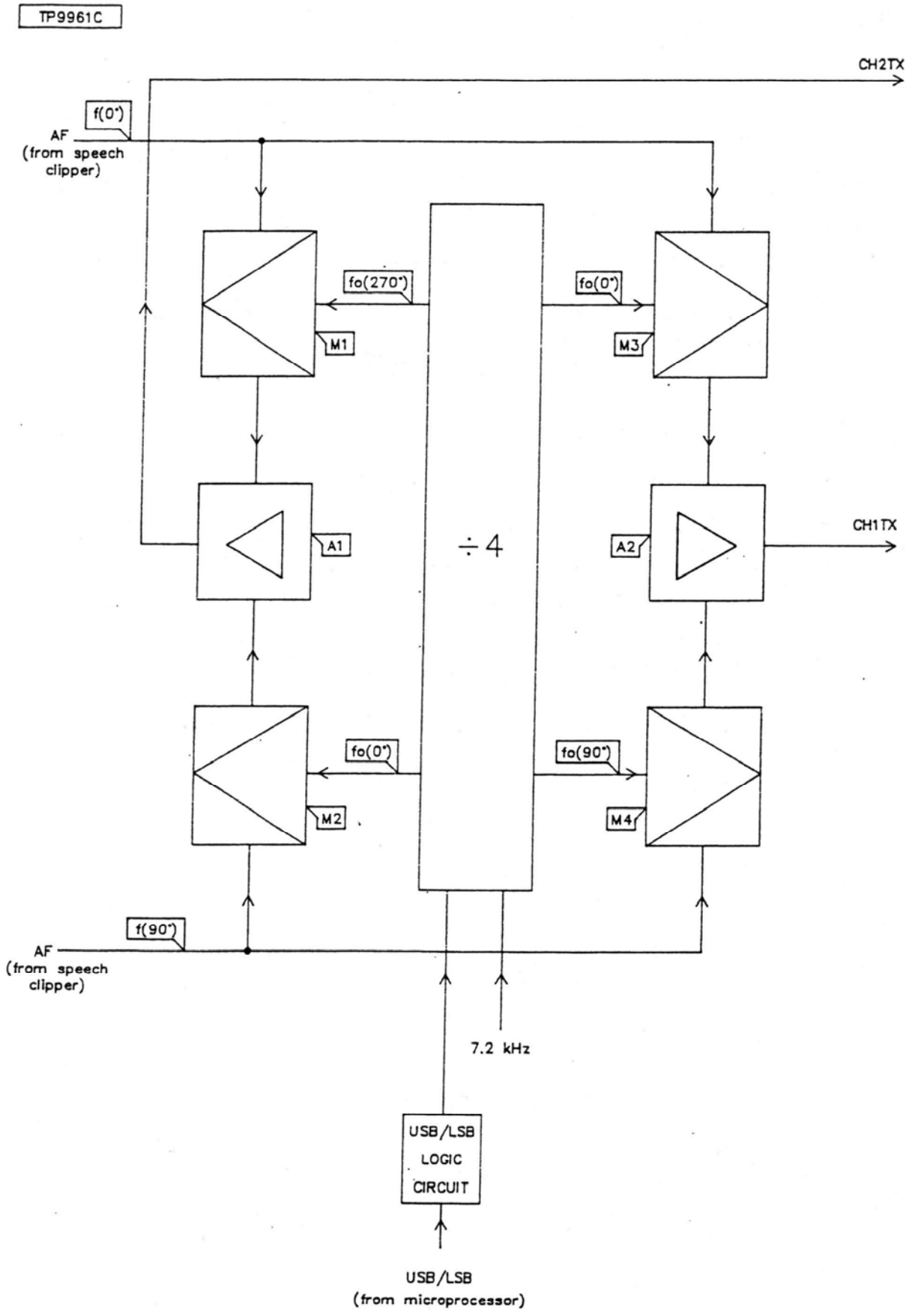
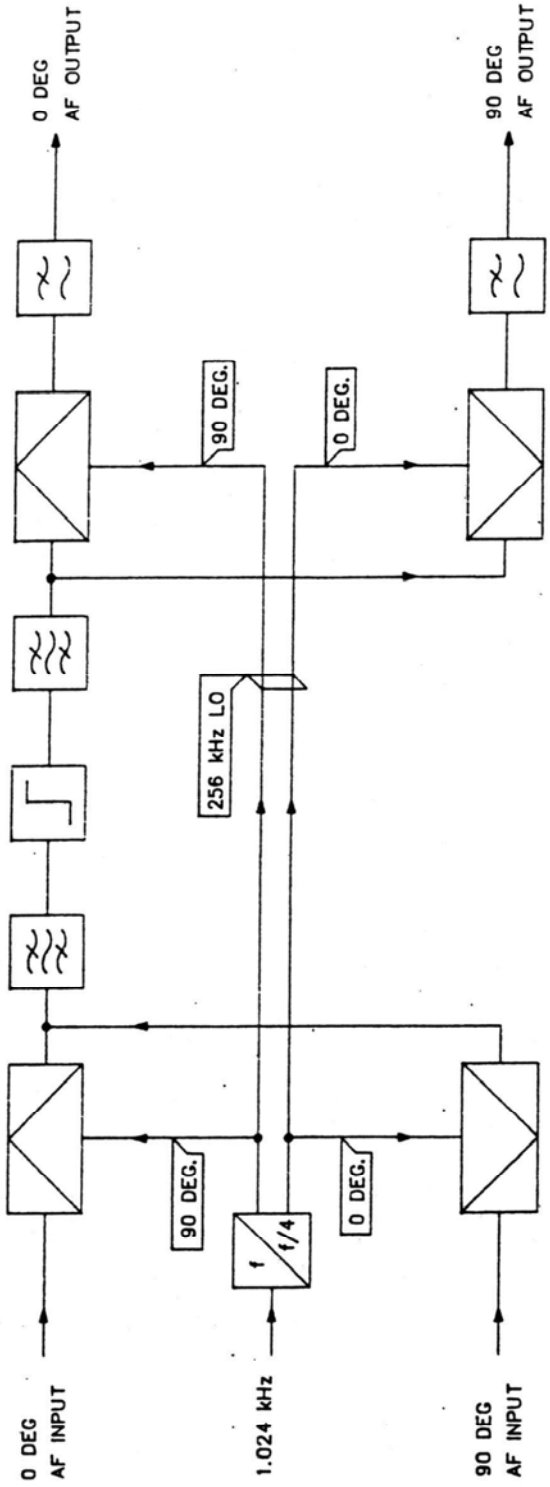


Fig 3.0.5 Transmit Modulators : Block Diagram



IP9955C

Fig 3.0.4 Speech Clipper : Block Diagram

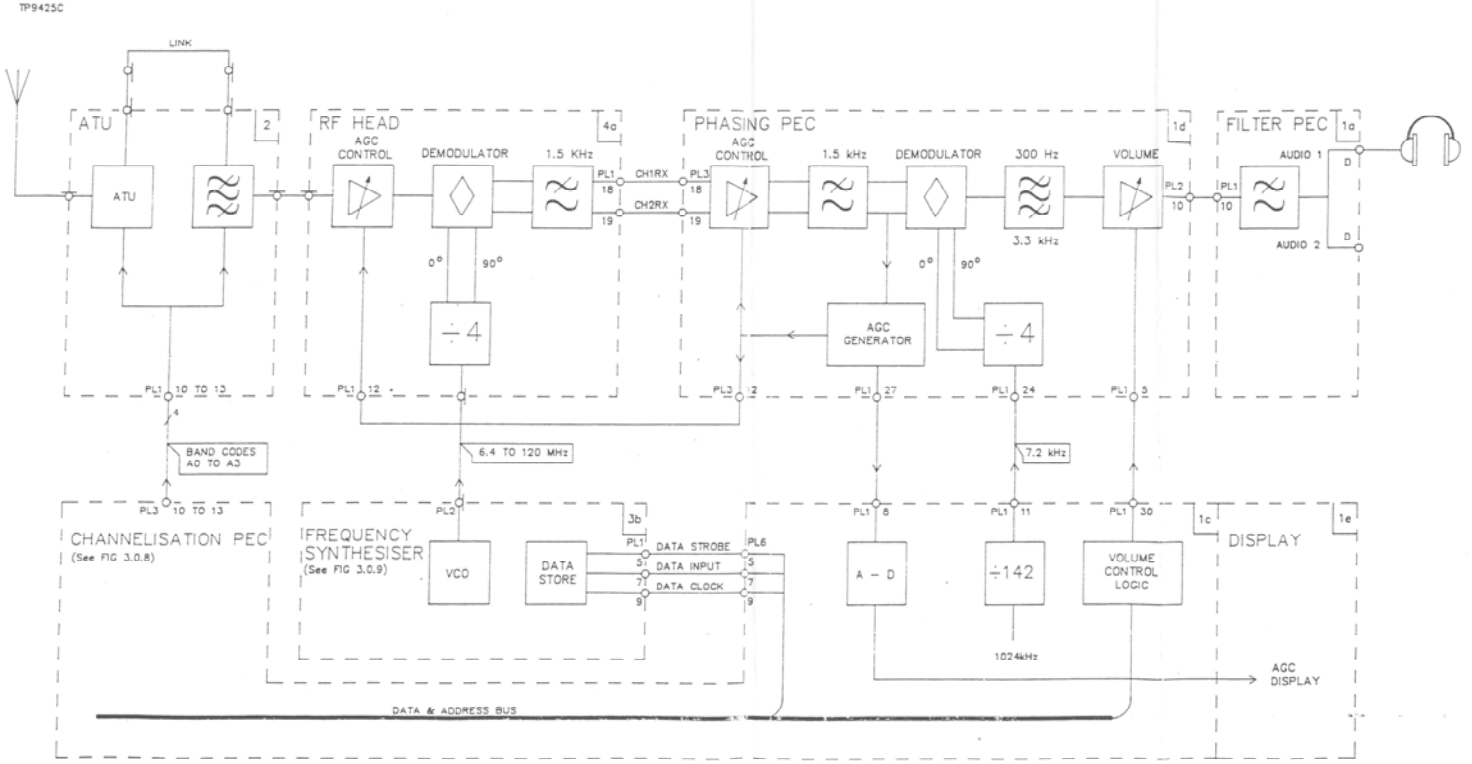


Fig 3.0.7 **Receive Mode : Block Diagram** **Fig 3.0.7**

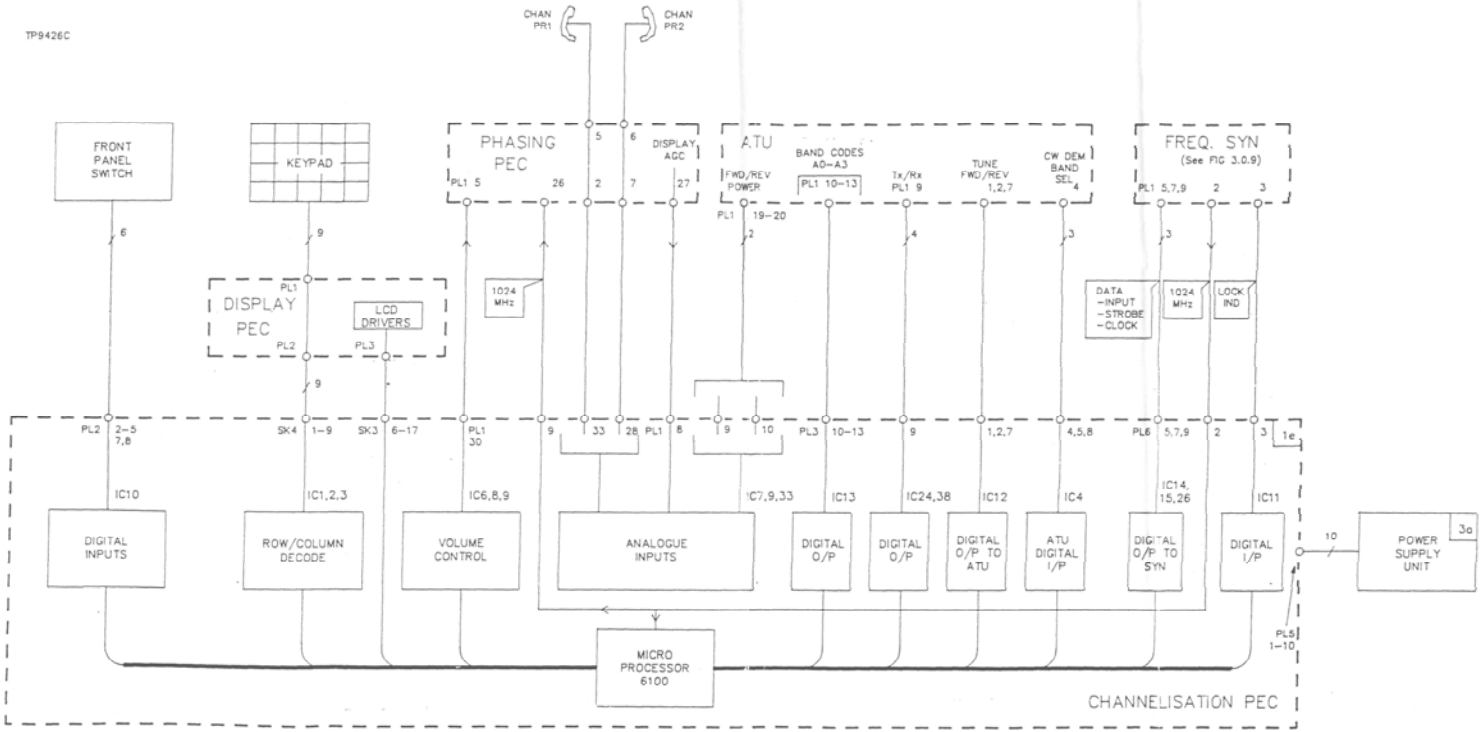


Fig 3.0.8 Channelisation : Block Diagram Fig 3.0.8

TP9474C

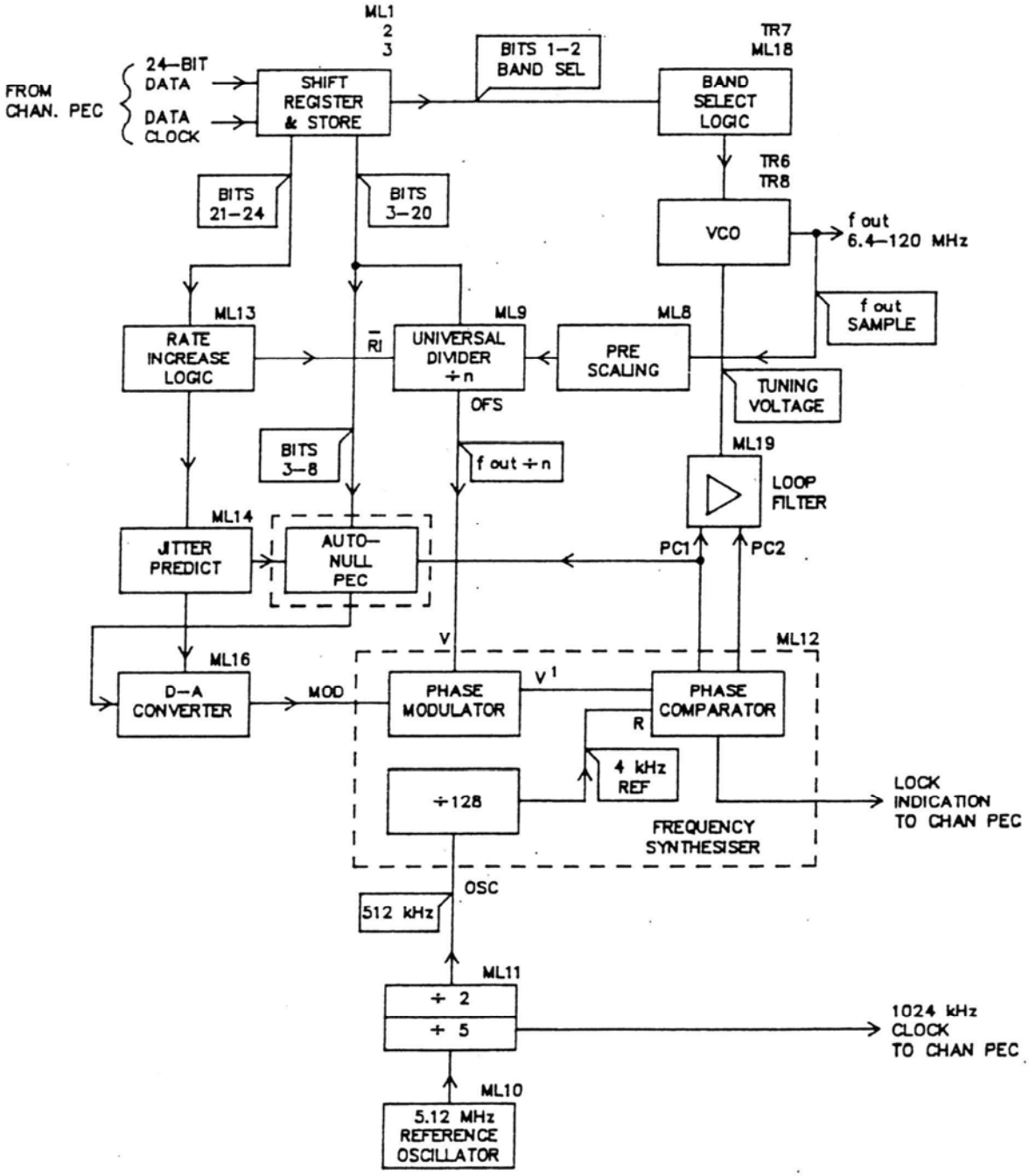
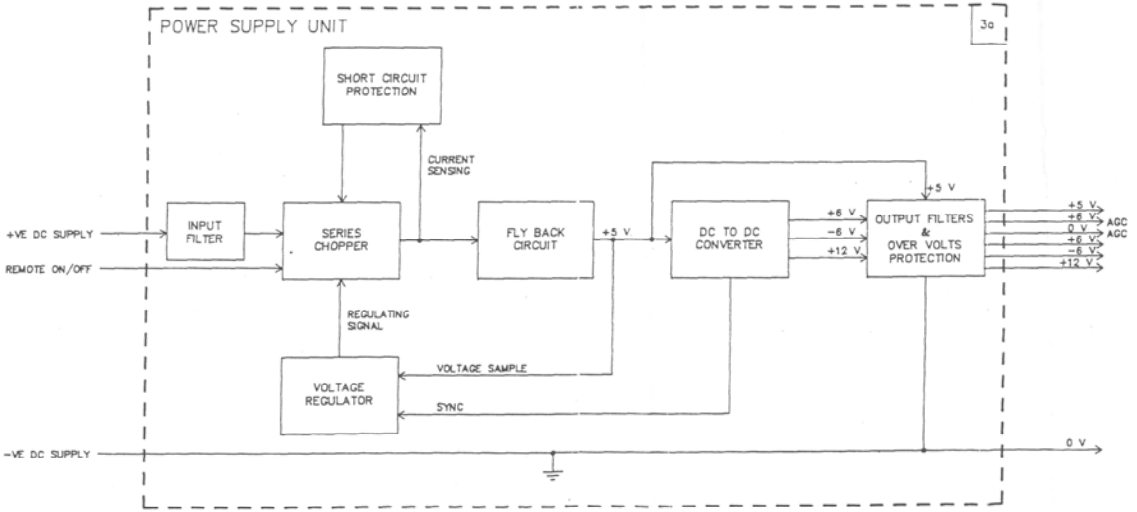


Fig 3.0.9 Frequency Synthesis : Block Diagram

TP9496C


POWER SUPPLY UNIT
3a
SHORT CIRCUIT PROTECTION
CURRENT SENSING
+VE DC SUPPLY
REMOTE ON/OFF
INPUT FILTER
SERIES CHOPPER
FLY BACK CIRCUIT
+5 V
DC TO DC CONVERTER
+6 V
−6 V
+12 V
+5 V
OUTPUT FILTERS & OVER VOLTS PROTECTION
+5 V
+6 V
0 V
AGC
AGC
+6 V
−6 V
+12 V
REGULATING SIGNAL
VOLTAGE SAMPLE
VOLTAGE REGULATOR
SYNC
−VE DC SUPPLY
0 V

CHAPTER 3.1

CHANNELISATION

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Illustrations

CHAPTER 3.1

CHANNELISATION

INTRODUCTION

1 Channelisation forms part of the case and sub-unit assembly (Fig 3.1.1 - Item 1ca) and consists of one PEC. A microprocessor, D-A converter and memory, all linked by an address/data bus to input and output buffers, enables Channelisation to:

(a) accept control inputs from the operator,

(b) store information,

(c) apply digital control to the remaining transmitter/receiver circuits.

2 The following description refers to the Channelisation circuit diagram (Fig 3.1.4) and is sub-divided into Initialisation, Keyboard entry, Control signals, Analogue inputs, 7.2 kHz clock and Battery backup sections.

INITIALISATION

3 When the transmitter/receiver is first switched on via the rotary switch on the front panel a RESET signal is fed to the microprocessor. This transfers control to an initialisation routine, stored in the read-only-memory (ROM), to ensure a controlled and consistent start-up. The $\overline{\text{RESET}}$ is generated by TR5, IC42/e and IC42/f after a time delay determined by R62 and C14. Following a further time delay set by R63 and C15 a RUN signal is generated from the $\overline{\text{RESET}}$ signal and fed to the microprocessor to start the initialisation sequence. The time delays allow the dc voltages in Channelisation to stabilise before initialisation starts. The RUN signal is also fed to IC24/c to enable Tx/Rx1 signal to be output to the antenna tuning unit on the command of the microprocessor. Although the initialisation sequence is stored in ROM, data required by the microprocessor to complete the sequence is stored in random-access-memory (RAM), IC19. The RAM is selected by the combination of line A13 and NAND gate IC28/a which produce a select signal, the value of which also depends on the $\overline{\text{RESET}}$ and output from TR5.

4 The microprocessor then executes a set of instructions in the initialisation routine, to determine the initial state of the transmitter/receiver as follows.

Option Format

5 For approximately two seconds the Display shows a code of ones and/or zeros (option format) to inform the operator of any special facility that is available in the Channelisation assembly. This routine is held in ROM so that the options are consistent. The microprocessor provides outputs for the Display as AD0 to AD7 signals on J3/6 to J3/9 and J3/14 to J3/17.

Display Light.

6 The Display light is switched off by setting to 5 V the AD0 input to the buffer IC13. This in turn switches off TR3 and TR4 and so interrupts the supply to the light on J3/4.

Low/High Power

7 Low power is selected by the microprocessor setting to zero the AD7 input to buffer IC38 causing a logic zero input to be applied to NAND gate IC24/a. The output of IC24/a is therefore set to logic one. This output is fed to Phasing to set the level of output power during transmit operations.

Receive Mode

8 The transmitter/receiver is switched into the receive mode by the microprocessor setting the correct values of Tx/$\overline{\text{Rx1}}$, Tx/$\overline{\text{Rx2}}$, and $\overline{\text{Rx CONN}}$ signals onto P1/14, P1/18 and P1/20 respectively. A logic zero on each of these lines is fed to the remaining PECs within the transmitter/ receiver, setting the circuits common to receive and transmit into the receive mode. The logic zeros are produced by setting to zero the AD0, AD1 and AD3 inputs to D-type flip-flop IC38. Immediately prior to the transmitter/receiver switching to the receive mode an alarm tone is triggered as detailed in the following paragraph.

Sidetone/Alarm

9 A sidetone/alarm of 1 kHz is produced by Channelisation from the 1.024 MHz clock input on J2/2. Frequency divider IC35 reduces the clock signal to 1 kHz before feeding it, via digital switch IC34/a to Phasing on P1/34. The initialisation sequence suppresses the sidetone/alarm by setting to zero the AD5 input to IC32, which puts a logic zero onto the enable input of IC34/a.

Calltone

10 A calltone is produced by Channelisation in the same way as the sidetone/alarm described in the previous paragraph. The only difference is that the calltone alternates between 0.5 and 1 kHz and is fed to Phasing on P1/32. Switching of the calltone between 0.5 and 1 kHz is achieved by the microprocessor enabling one of two digital switches IC34/b and IC34/c. Suppression of the calltone by the initialisation sequence is effected as for sidetone by setting to zero the AD3 and AD4 inputs to IC32.

Volume

11 The level of the audio signal is usually set by operation of the keyboard '+' or '-' keys. The microprocessor decodes the input as described in para 14 and produces AD0 to AD5 input signals for D-type flip-flop IC6. D/A converter IC8 then produces an analogue signal equivalent to the digital output from IC6. This signal is amplified by IC9/a and b before being fed to Phasing via P1/30. In the initialisation routine the microprocessor produces logic values for AD0 to AD5 to give an intermediate level of audio signal.

Synthesiser Lock

12 The operating frequency of the transmitter/receiver is provided by the Synthesiser from programming data produced by Channelisation. This data is generated by the microprocessor as a series of logic inputs fed via AD7 to a latch IC14. A voltage converter IC15c then changes the voltage level of the data from 5 V to 12 V before the data is fed to the Synthesiser via J2/7. When the transmitter/receiver is first switched on the data generated by the microprocesor is determined by the frequencies previously stored in the RAM. The initialisation routine then checks that synthesiser lock has been achieved by monitoring the LOCK IND signal on J2/3. If

a logic zero 'LOCK IND' signal is fed, via latch IC10 and signal AD1 to the microprocessor, no further action is taken. If a logic one 'LOCK IND' signal is received, indicating that synthesiser lock has not been achieved, the microprocessor enables the alarm tone (para 8) and programs AD0 to AD7 outputs (J3/6 to J3/9 and J3/14 to J3/17) to give a 'PH' warning on the Display, indicating that the Synthesiser is 'out of lock'.

Battery Voltage Check

13 The battery voltage (level) is checked by comparing the actual voltage present with a digital representation of the minimum required level. The supply voltage is fed to Channelisation on P2/9 (BATT SW) where it is applied to multiplexer IC33 along with five other analogue signals. Programming logic, produced by buffer IC32 from inputs AD0 to AD5 generated by the microprocesor, selects the required output from the multiplexer and feeds it to the comparator IC9/c. The microprocessor then generates AD0 to AD3 signals for buffer IC5, the value of the signals being equivalent to the minimum voltage level required. The digital output from IC5 is converted to an analogue signal by D/A converter IC7 and fed to comparator IC9/c. If the battery voltage is above the minimum value required, the output from the comparator is zero and no further action is taken. If the voltage is below the minimum value required, the comparator produces an output which is fed to the microprocessor via latches IC10. This in turn causes the microprocessor to enable the alarm tone (para 7) and program AD0 to AD7 outputs (J3/6 to J3/9 and J3/14 to J3/17) so that when they are received by the Display a 'BA' warning is shown, indicating that the battery voltage is low.

Display

14 The final action taken by the initialisation routine is to set up the Display to show the current frequency, mode and channel. To achieve this the microprocessor programs the AD0 to AD7 outputs on J3/6 to J3/9 and J3/14 to J3/17 according to information entered via the keyboard (para 14).

KEYBOARD ENTRY DETECTION

15 When a key is pressed it makes a connection between the row and the column of the key in question, ie if the key positioned at row two column three was pressed, a connection would be made between row two and column three of the keyboard. The microprocessor successively activates each row by programming AD0 to AD3 inputs to latch IC1 and digital switch IC2. With one row activated the state of each column is read by the microprocessor via buffer IC4. Therefore, taking the example above, when row two is activated (ie logic one) by IC1 and 2 the key depression will switch the logic one to the column three input of IC4. In this way the microprocessor can determine which key was pressed by monitoring AD0 to AD3 inputs to IC1 and AD0 to AD4 outputs from IC4. The correct sub-routine can then be executed according to the entry made.

CONTROL SIGNALS

16 Apart from the inputs and outputs already mentioned (AD0 to AD7 and D0 to D3) the microprocessor also generates four further control signals. These signals are necessary because of the use of a common address and data bus. The functions of these signals are as follows:

(a) ALE : Determines the moment at which the address is present on the bus.

(b) $\overline{RD}$: Indicates that data is to be read.

(c) $\overline{WR}$: Indicates that data is to be written.

(d) IO/$\overline{M}$: Addresses the memories, ROM and RAM, and i/p and o/p devices.

17 All the inputs and outputs to and from the microprocessor are fed through input and output buffers or latches. The selection of each device is performed by read strobes $\overline{SR0}$ to $\overline{SR3}$, and write strobes $\overline{S0}$ to $\overline{S15}$.

Read Strobes

18 The read strobes $\overline{SR0}$ to $\overline{SR3}$ are produced by demultiplexer IC31 from information generated by the microprocessor. Processor outputs IO/$\overline{M}$ and $\overline{RD}$ are decoded by inverter IC27 and exclusive OR gate IC21 to produce an enable signal for IC31. At each enable signal, the state of the read strobes $\overline{SR0}$ to $\overline{SR3}$ is determined by the multiplexer inputs A0 and A1. Note that strobes $\overline{SR0}$, $\overline{SR1}$ and $\overline{SR3}$ are used within Channelisation, while $\overline{SR2}$ is used externally, via P4-9.

Write Strobes

19 The write strobes $\overline{S0}$ to $\overline{S15}$ are produced by demultiplexer IC26 from information generated by the microprocessor in the same way as the read strobes except that processor outputs IO/$\overline{M}$ and $\overline{WR}$ are decoded to produce the enable signal for IC26. Strobes $\overline{SO}$, $\overline{S1}$ and $\overline{S2}$ are inverted by IC27 to produce external strobes S0, S1, S2.

20 The following additional strobes are also generated for use elsewhere in the transmitter/receiver:

(a) $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$, fed to the Display via inverter IC27.

(b) $\overline{S5}$ and $\overline{S6}$, passed through the inverters IC27/a and b and the 5 V to 12 V voltage converter IC15/a and b before being fed to the Synthesiser as DATA STROBE and DATA CLOCK respectively.

(c) $\overline{S12}$ and $\overline{S13}$, not used.

ANALOGUE INPUTS

21 The following analogue signals are fed to Channelisation on P1/33, P1/28, P1/20, P3/19 and P1/8 pins respectively:

(a) CH/PR1 (channel change/pressel 1)

(b) CH/PR2 (channel change/pressel 2)

(c) FWD PWR (forward power)

(d) REV PWR (reverse power)

(e) AGC DISPL (automatic gain control display)

Each signal is applied to IC33 and measured in the same way as the battery voltage check detailed in para 12.

7.2 kHz CLOCK

22 A 7.2 kHz clock signal is produced by Channelisation for use in the Phasing modulating/demodulating circuit. The 1.024 MHz clock signal from the synthesiser assembly is fed to Channelisation on J2/2 and applied to the clock input of the divider formed by the combination of down counters IC36 and IC37. The output from the divider (7.212 kHz) is passed to Phasing via P1/11.

BATTERY BACKUP

23 To maintain the contents of the RAM during loss of power, ie change of main battery, a battery backup circuit is provided. With the main battery connected a 15 V supply is present at P2/1 (BATT) and is applied to the RAM via R67, D12 and R66. At the same time the internal battery is recharged. When the BATT input is removed the internal battery supplies a trickle current to the RAM. TR6 and TR8 form a voltage regulator to keep the voltage applied to the RAM at a constant level.

Note: If lithium batteries are fitted, the trickle charge is not maintained.

OPTIONS

24 The Table 3.1.1 shows the options available. The links are situated on the Channelisation board and may be located by reference to Fig 3.1.3.

Table 3.1.1 Options Available

LINK		
POSITION	1 (OPEN)	0 (CLOSED)
1	3rd Rom Fitted	
2	Not Allocated	
3		Memory Protection
4	CCIR	FINABEL

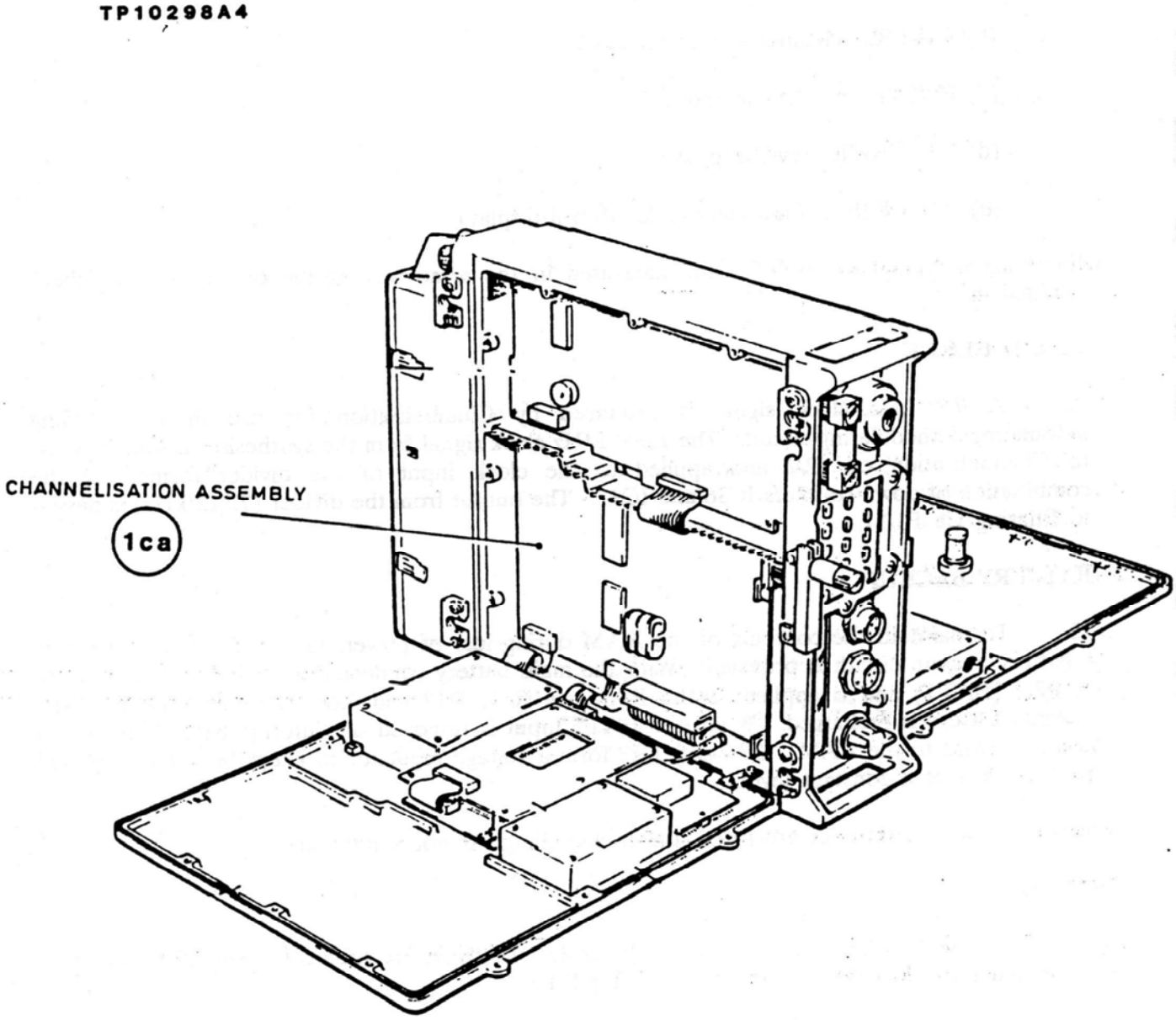

Fig 3.1.1 Channelisation PEC Location

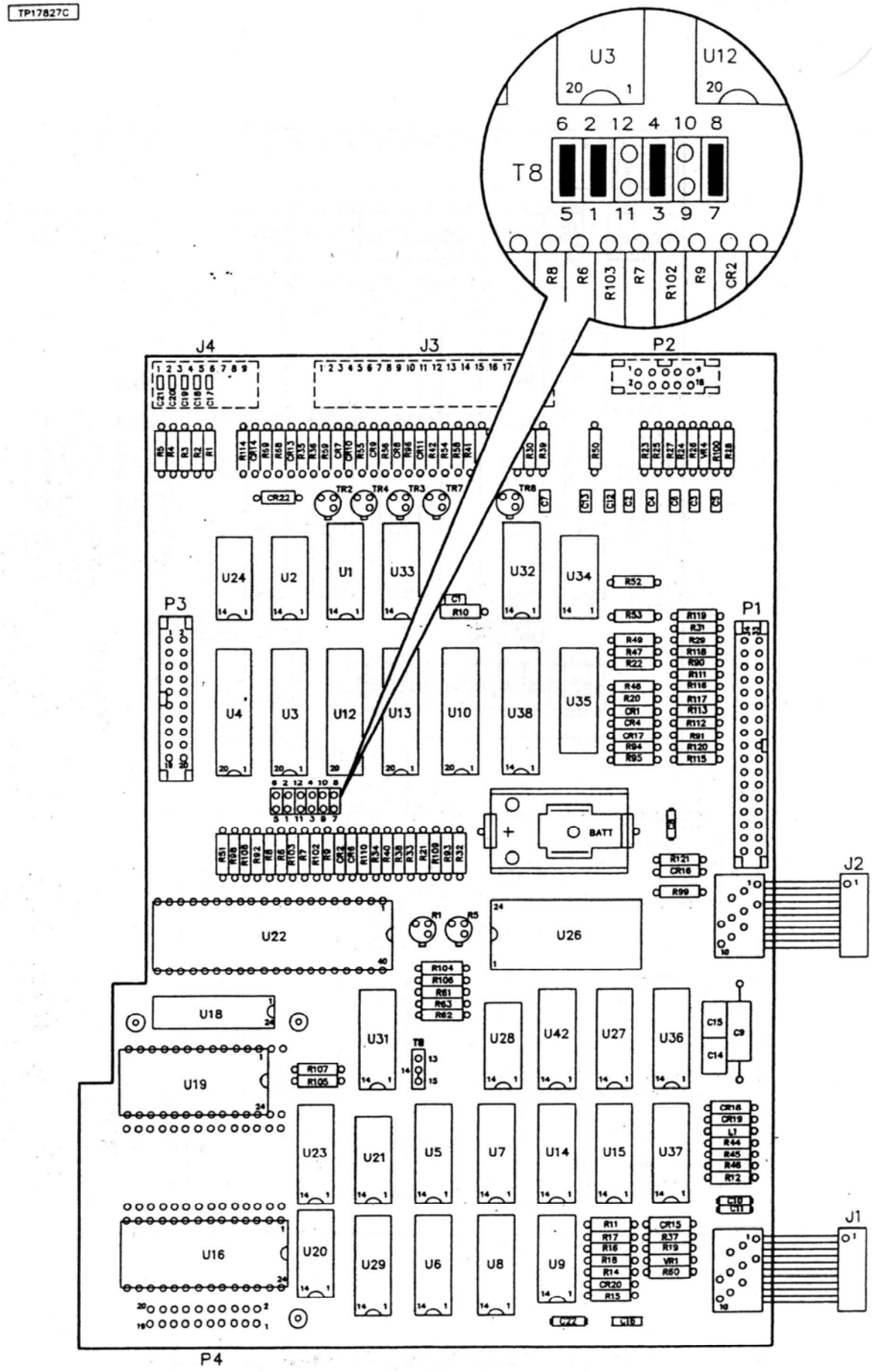

Fig 3.1.2 Scrap Detail of Channelisation PEC Showing Link Details

TP17828C

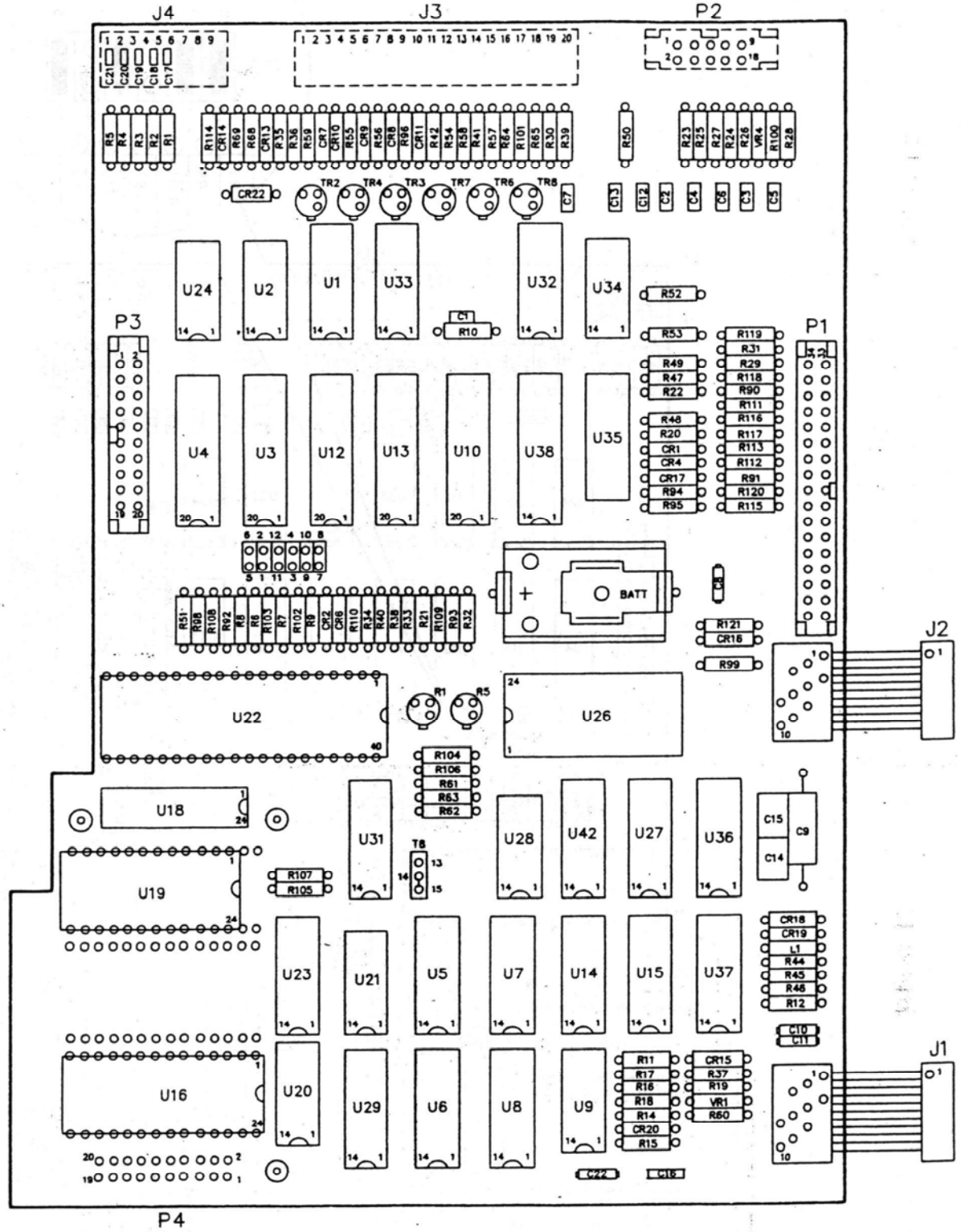

Fig 3.1.3 Channelisation PEC Component Location

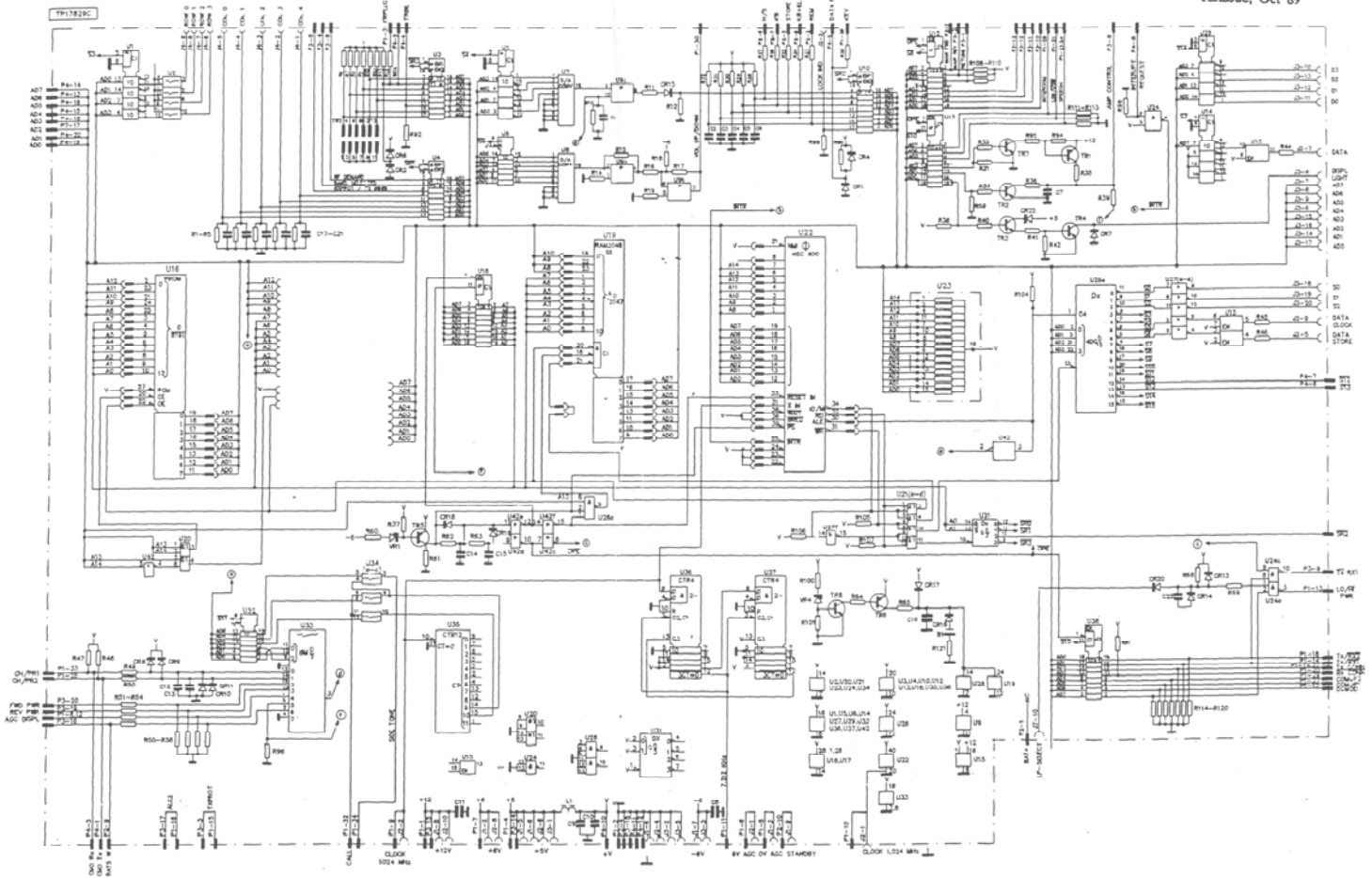

Fig 3.1.4 Channelisation Circuit Diagram Fig 3.1.4

CHAPTER 3.2

PHASING

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CHAPTER 3.2

PHASING

INTRODUCTION

1 Phasing forms part of the case and sub-unit assembly (Fig 3.2.1 - Item 1d) and consists of one PEC. The following description refers to the Phasing circuit diagram (Fig 3.2.3, Sheets 1 to 6) and is broken down to Receiver, Transmitter and Tx/Rx switching functions.

RECEIVER

2 The two folded-over audio signals from the RF Head (Rx CH1 and Rx CH2) are fed to Phasing on P3/18 and P3/19 (Fig 3.2.3, Sheets 1 and 2). The signals follow similar paths through the Phasing up to IC40 (para 13), the only difference being that Rx CH2 is sampled by the automatic gain control (AGC) voltage generator circuit. The following text (para 3 to 12 inclusive) explains the signal path for Rx CH2. This text can also be used for Rx CH1 signal path by changing the component numbers and ignoring the AGC voltage generator explanation (paras 5 to 7 inclusive).

Automatic Gain Controlled Amplifier

3 Rx CH2 signal is applied to P3/19 where the values of C2 and R2 are closely matched to the values of C1 and R1 (Rx CH1) so that the phase and attenuation characteristics of both channels are balanced. The received signal is then fed to two series automatic gain controlled amplifiers (IC2 and IC3) via dc blocking capacitor C8. The gain of each amplifier is determined by the AGC current, produced by the AGC voltage generator (paras 5 to 7) and interface circuit (paras 9 to 11), which is fed to pin 16 of ICs 2 and 3. Control of the overall gain of the amplifier stage is also available by means of variable resistors R20 to R24. Matching of the two channels prior to the application of AGC current is achieved by R22 to R24, while the gain of both channels is matched over the total AGC range by R20 and R21.

Note: IC1 is a logic switch that 'grounds' the input channels when the radio is operating in the Transmit mode.

4 DC negative feedback is applied to both amplifiers via R8, R10 and R14, R16 respectively, thus keeping the dc gain very low. AC feedback is also applied to both amplifiers via C12 and C18 respectively. The output of IC2 is ac coupled to IC3 by C14 before the final amplified signal from IC3 is fed to the next stage within Phasing (Filter Network, para 12). A sample of this output is also fed to the AGC voltage generator via TB20 and TB21.

AGC Voltage Generator

5 The sample taken from the output of IC3 is applied to the AGC voltage generator (IC4) via variable resistor R42, which sets the input threshold, and an audio coupling capacitor C28. IC4 consists of an input af amplifier coupled to a dc output amplifier by means of two detectors. The time constants of the detectors are set by capacitors C25, C26, C27 C160, C161 and C162. Application of an af signal on pin 1 of IC4 establishes an AGC voltage level output at pin 2. If the input signal rises above the charging threshold set by R42/C28 a trigger circuit is activated

whose output pulses provide a discharge current for C25 and C26. This allows the voltage present at pin 3 to decay at a maximum rate, causing the output voltage at pin 2 to fall and follow smoothly the received af signal.

6 If the received af signal should fade quickly or disappear completely (pauses in speech) the input to IC4 falls below the threshold level. This causes the trigger circuit to deactivate allowing C25 and C26 to hold their charge and keep the AGC voltage (Pin 2) at the same level. If after a certain interval (t1) no further af signal is received the AGC voltage falls to a minimum, restoring full receiver gain. This is achieved as follows: the duration of t1 is set by selecting into circuit capacitors C23, C24 and C167. When data reception line H to the gate of TR1 is LOW, C23 and C24 are not in circuit, so t1 is set by C167 only. For speech reception, line H goes HIGH switching C23 and C24 into circuit so that t1 is dependent on all three capacitors. This results in a much longer interval for speech reception than for data reception. When the trigger circuit is active (para 5) it charges the selected capacitors via limiting resistor R31. With the trigger circuit deactivated the capacitors discharge in time t1, after which C25 and C26 are also discharged rapidly, reducing the AGC voltage to a minimum. If an af signal is received within the interval (t1) the capacitors connected to pin 6 of IC4 recharge and restore the AGC voltage.

7 To ensure that full receiver sensitivity is attained when switching from transmit mode to receive mode, C25 and C26 are discharged under transmit conditions by TR2, which is switched ON by line B going HIGH (transmit).

Comparator

8 The output produced by the AGC voltage generator is fed to the AGC controlled amplifiers on the RF Head via a comparator (IC42). The comparator produces a dc output proportional to the AGC voltage applied via potential divider network R256 and R257. A reference voltage of +6 V is also applied to the comparator via potential divider network R259 and R260. As the gain of the comparator is approximately 60, the output is 60 times the difference between the input (AGC voltage) and the +6 V reference.

Interface Circuit

9 The interface circuit converts the AGC voltage generated by IC4 into a current source to control the gain of IC2 and IC3 (paras 3 and 4). The circuit consists of TR3, IC6, IC5 and associated components and operates as follows.

10 TR3 is a pair of matched transistors having very high current gain and low noise operation. The left-hand transistor is biased on by the fixed base bias of R37 and R40. Pin 3 of IC6 is always at +1 V dc because of the potential divider network R38 and R39. Therefore the circuit TR3 and IC6 stabilises at a point where the voltages at IC6 pins 2 and 3 are equal ie +1 V dc. As the AGC voltage increases it switches the right-hand transistor of TR3 ON (the current source for this transistor being provided by IC5). As the collector current of the right-hand transistor increases, the voltage at IC5 pin 2 falls. This causes the voltage at IC5 pin 6 to increase, driving more current through the current sharing network of R43 and R44 to the AGC controlled amplifiers IC2 and IC3.

11 An increase in the collector current of the right-hand transistor of TR3 also results in an increase in current through the emitter resistor R36, causing the left-hand transistor of TR3 to switch OFF. The voltage present at pin 2 of IC6 therefore rises above the reference level at

pin 3. Pin 6 of IC6 goes negative and allows the increase in TR3 emitter current to flow through R36. This means that the left-hand transistor current remains constant keeping the TR3 emitter voltage constant. The gain of IC6 is very high, so a small difference in voltage between pins 2 and 3 of IC6 causes a large change in output voltage. Therefore any increase in AGC voltage generated by IC4 will result in a large increase in the current supplied to the AGC controlled amplifiers, IC2 and IC3.

Filter Network

12 As stated in para 4, the amplified af signal from IC3 is fed to the filter network which consists of three low noise operational amplifiers (op amps). The amplifiers are ac coupled to IC3 by capacitor C20 and are configured as an active low-pass filter with unity gain and zero dc at the output (IC12 pin 6). Each of the op amps is supplied with +6 V AGC supply for noise immunity.

Demodulator

13 The outputs from the filter networks of both channels (IC11 pin 6 and IC12 pin 6) have a 90° phase difference, and are fed to the balanced demodulators (IC16 and IC17) via logic switch IC40. Because the received af signals Rx CH1 and Rx CH2 can represent either a lower sideband (lsb) or an upper sideband (usb) signal, the phase of the demodulating signal fed to the demodulators must change according to the selection made on the keyboard (LSB or USB). This change in phase is achieved by a phase determination network, IC20 and IC21. Phasing receives a lsb/usb selection signal from Channelisation via P1/14. IC20 and IC21 convert this input to three programming logic signals for the frequency divider IC19. A 7.2 kHz reference signal from Channelisation is fed to pin 9 of the frequency divider via IC21. The correct frequency (1.8 kHz) and phase relationship of the outputs from IC19 are therefore maintained for the particular sideband selected.

14 The outputs from the demodulators are combined in IC18 to produce an unfolded true audio spectrum signal. Provided that the unit is operating in the receive mode, IC41c allows this signal to pass on to the same filter chain as used in the transmit mode (para 19). The filtered output from IC32 pin 14 is then fed to IC41b/d. When IC41d is selected into circuit, IC41b/d acts as an attenuator so that the received input is heard as a background signal (intercom). For the purpose of this description it is assumed that IC41b/d has no effect on the audio input. Following IC41b, a pair of voltage controlled amplifiers (IC36) boost the signal to a level determined by the control voltage (VOL UP/DOWN) from Channelisation. The af signal is then output to the filter assembly via the final amplifier stage IC37, TR7, TR8 and TR9.

Alarm

15 An alarm tone of 1 kHz is generated by Channelisation if any of the following fault conditions arises:

(a) Synthesiser out of lock

(b) Battery voltage low

(c) Rotary switch set to STORE or REM.

The tone is fed to Phasing via P1/1 and coupled to the sidetone circuit (para 17) via C137 and R235.

TRANSMITTER

16 The audio input signal is fed to Phasing via either P2/1 (µP1) or P2/2 (µP2). The following text explains the signal path for µP1 although the text can also be used to describe µP2 by changing the component numbers.

17 When the pressel is activated a logic '1' (+5 V) signal appears at P1/8 (COM µP1) enabling logic gate IC33. This allows the audio signal present on P2/1, which is amplitude limited by diodes D8 and D9, to be fed through to the pre-amplifier stage IC35. The output from IC35 follows two signal paths, sidetone via C138 and R234, and transmit via R218. The sidetone signal is fed to a pair of voltage controlled amplifiers (IC36) where the signal level is set by the control voltage (VOLUME UP/DOWN) from Channelisation. Following this amplification the sidetone is fed to the filter assembly via final amplifier stage IC37, TR7, TR8 and TR9, while the transmit signal is applied to a voice operated gain adjusting device IC34.

Voice Operated Gain Adjusting Device (VOGAD)

18 Application of the audio input to the VOGAD ensures that a constant modulating signal level is maintained for varying microphone output (ie varying speech level). When the unit is operating in the transmit mode a +6 V supply is fed to the VOGAD via TR4. The VOGAD uses an AGC loop to return its output to within 10% of its original level. The time taken to achieve this is determined by C129. TR10 on the output of the VOGAD buffers the IC34 output as it is switched by logic gate IC41 to the filter network IC32. IC41 is enabled by a transmit signal from Channelisation received on P1/16.

Filter Network

19 The filter network consists of four filters, all contained within IC32, providing an audio pass bandwidth of .3 to 3.3 kHz. After filtering, the audio input is fed to the speech processing circuit via C123.

Speech Processing

20 The speech processing circuit, which consists of IC26 to IC31, is used to increase the average power of the audio signals. First the signal is split into two equal paths at the junction of R135, R136 and R144 before being amplified by IC22 and IC23. Modulators IC24 and IC25 then produce outputs that are equal in amplitude but 90° out of phase. This is achieved by mixing the audio frequencies with a 256 kHz carrier (derived from the 1.024 MHz clock input on P1/26 via IC27 divide-by-four flip-flop). The outputs from the modulators are cross-connected and combined at T1 to give a single sideband i.f. signal at 256 kHz. This signal has its peak to mean ratio reduced in a clipper circuit (IC26), and the transformer-coupled input to and output from this circuit are tuned very precisely to give the required channel definition and equality. The output of IC26 is demodulated by IC28 and IC29 (using the same 256 kHz carrier) to produce two audio signals in quadrature. These are amplified in IC30 and IC31, and then fed via logic switch IC39 to the next modulation stage. During data operations the speech processing circuit is bypassed by IC39a and b, the output of IC22 and IC23 being fed direct to the modulator stage.

Modulator Stage

21 The purpose of the modulator stage is to produce two 'folded' quadrature signals with suppressed image sidebands. AC coupling of the speech processing circuit to the two pairs of balanced modulators (IC13, 14 and IC16, 17) is performed by capacitors C64, 65 and C68, 69. The outputs from the speech processing circuit are fed to two similar channels within the modulator stage (the only difference being that the phases of the signals change and the outputs of the modulators in channel one are subtracted while those in channel two are added). To avoid confusion the following text (to the end of para 22) applies for AFTxCH2 output (P3/14). The text can also be used to describe AFTxCH1 by changing the component numbers and subtracting the outputs of the modulators.

22 IC16 and IC17 are balanced modulators each receiving one of the two outputs from the speech processing circuit. The modulators also receive a carrier frequency of 1.8 kHz whose phase is determined by the selection of LSB or USB on the keyboard. The production of this carrier is described in para 13. When the outputs from IC16 and IC17 are combined in IC18 a 'folded' single sideband (ssb) signal is produced. 'Folded' effect is achieved by ensuring that the carrier frequency lies in the centre of the audio spectrum and means that all the original information is contained within a bandwidth of half the audio input. The ssb signal is produced by selecting the phase of the carrier so that when the outputs of the modulators are added, the unwanted sideband is subtractive and cancels out while the required sideband is additive and is reinforced.

23 The two 'folded' af quadrature phase related signals are then fed out to the RF Head as AFTxCH1 and AFTxCH2 via logic switch IC40.

TX/RX SWITCHING

24 Some of the receive and transmit signal paths on the phasing assembly are common, eg filter network and modulator/demodulator stage. To ensure that the correct circuits are selected, the channelisation assembly supplies the phasing assembly with the following control signals:

(a) Tx/Rx 1 (P1/21)

(b) $\overline{\text{Rx CONN}}$ (P1/15)

(c) Tx CONN (P1/16)

These three inputs are converted to the eight control signals (A to H) required in Phasing by IC38, 43 and 44.

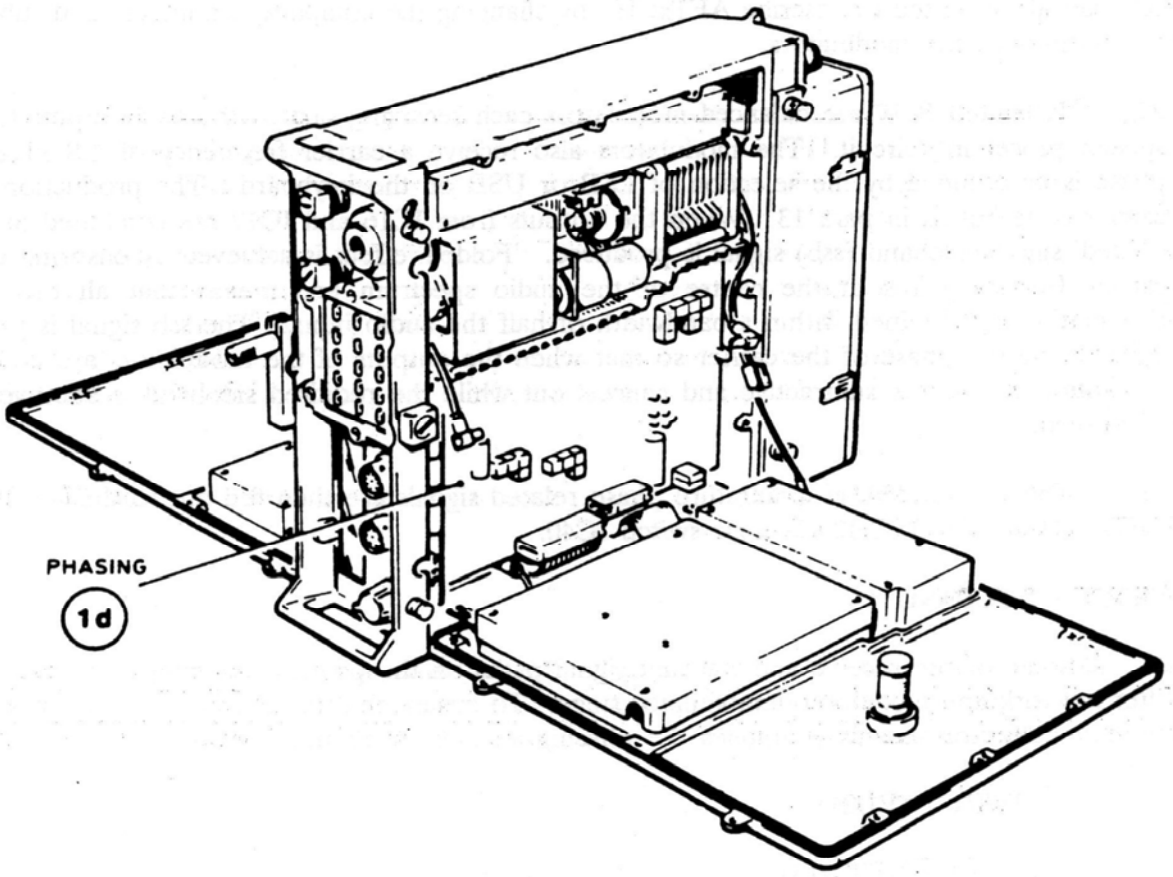

Fig 3.2.1 Phasing PEC Location

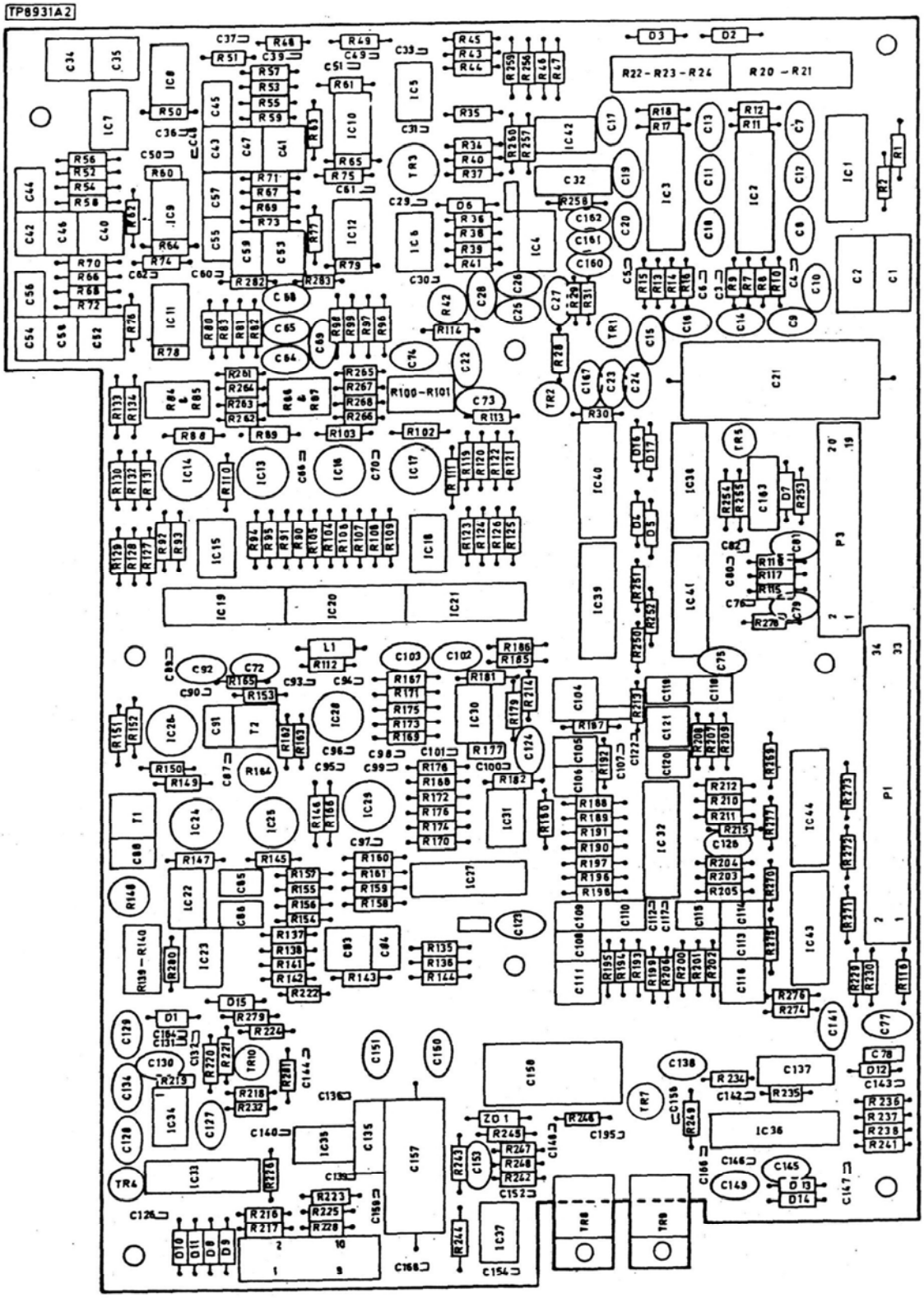

Fig 3.2.2 Phasing PEC Component Location

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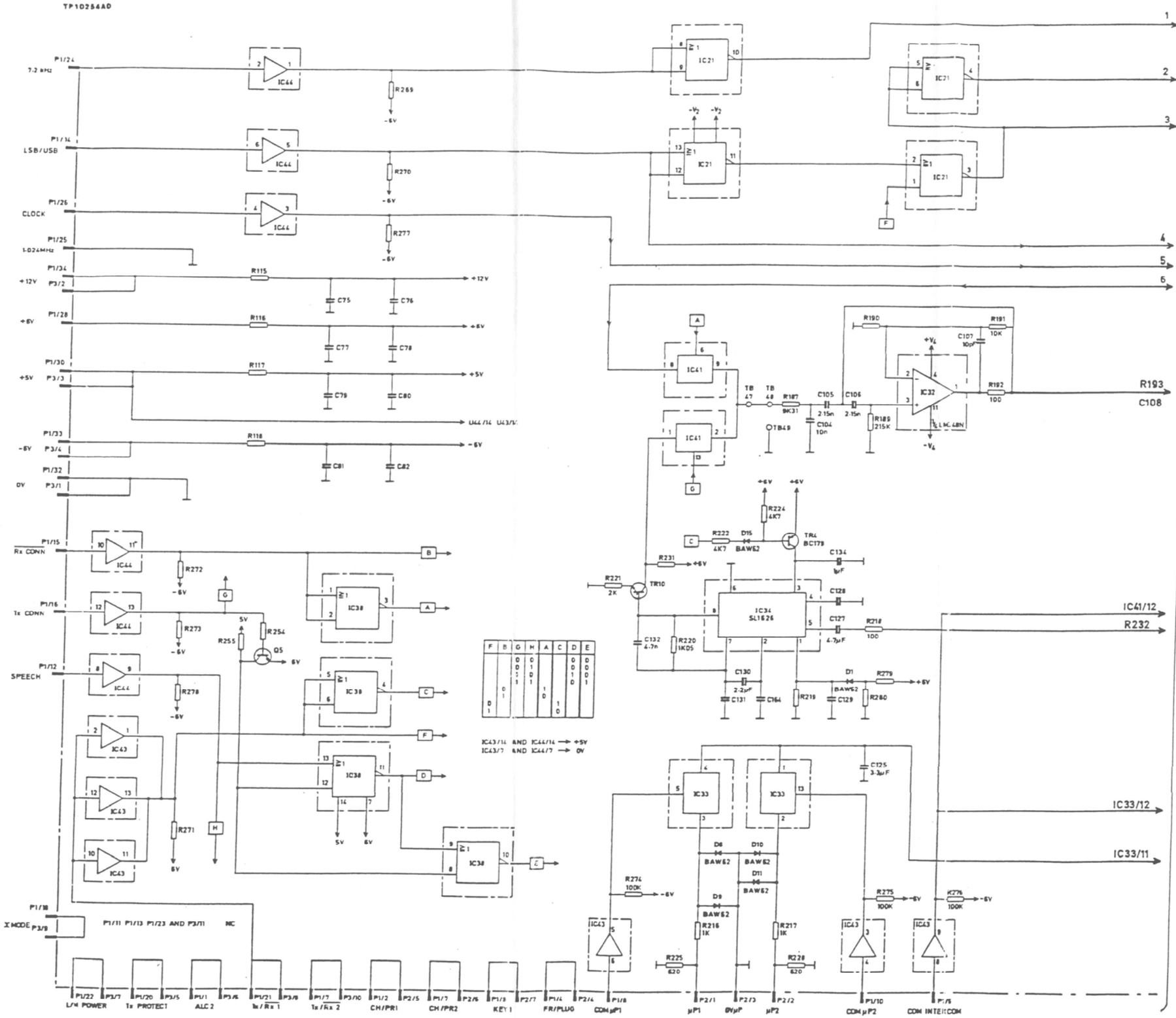
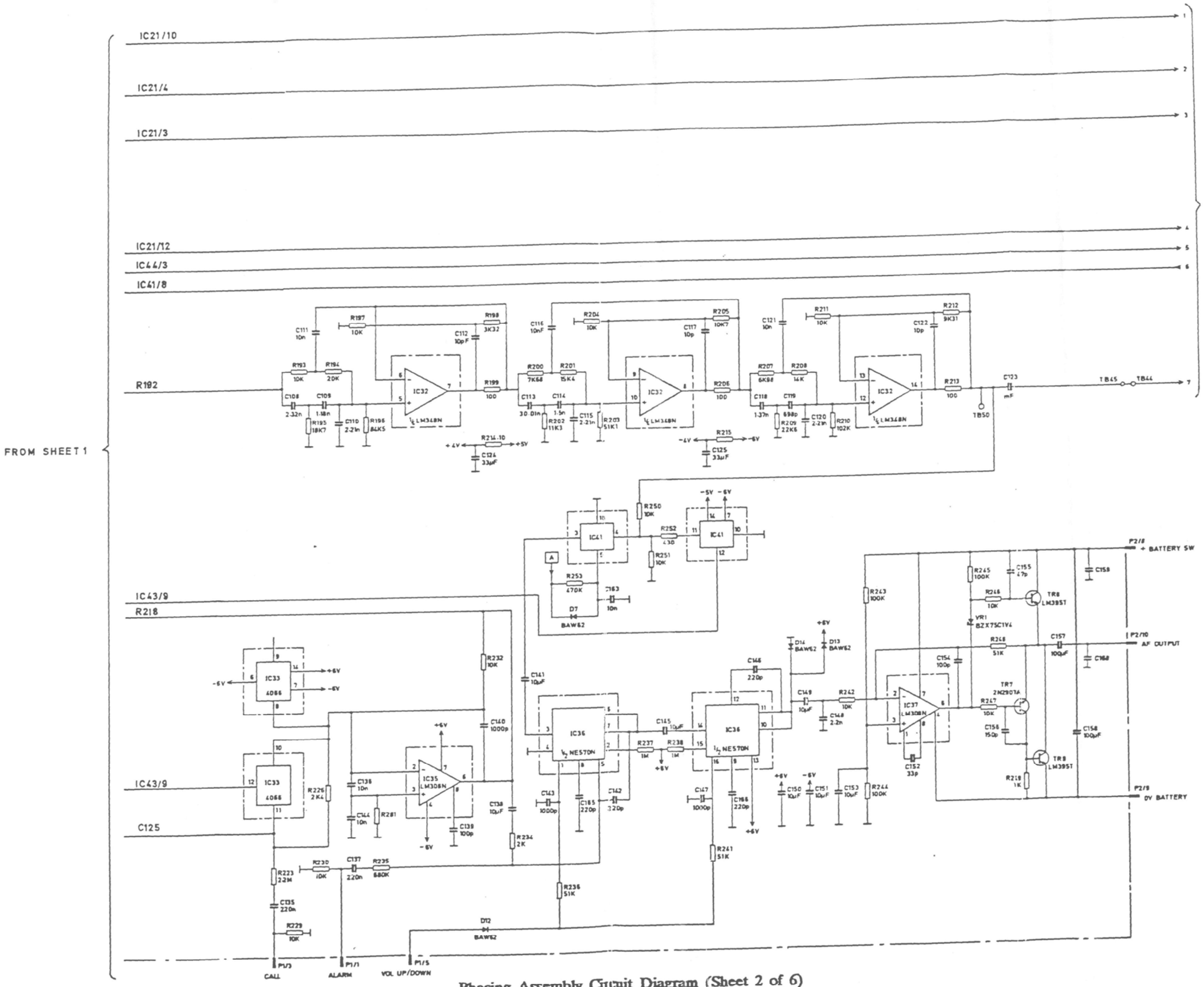


Fig 3.2.3

Phasing Assembly Circuit Diagram (Sheet 1 of 6)

Fig 3.2.3



Phasing Assembly Circuit Diagram (Sheet 2 of 6)

Fig 3.2.3

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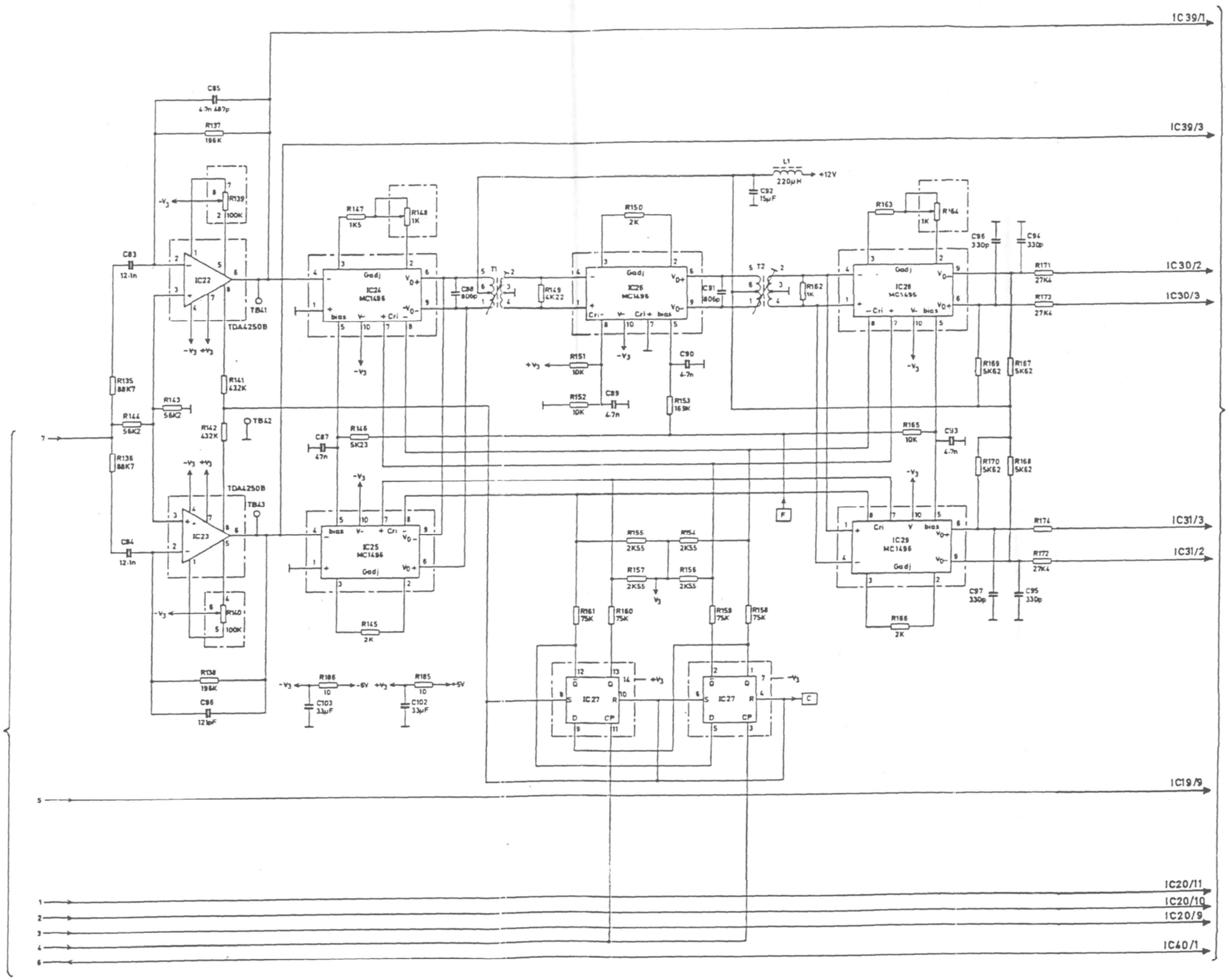


Fig 3.2.3 Phasing Assembly Circuit Diagram (Sheet 3 of 6) Fig 3.2.3

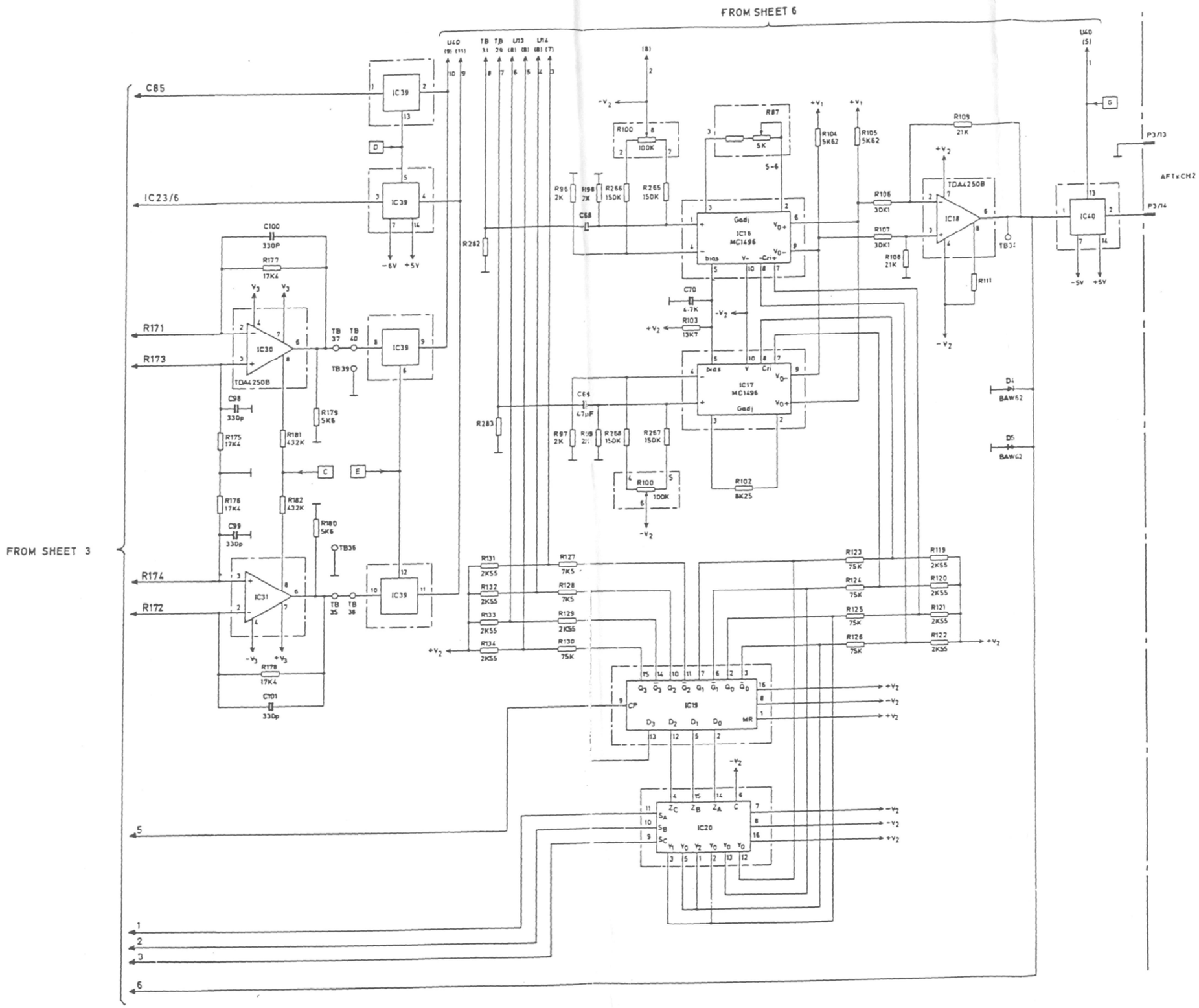
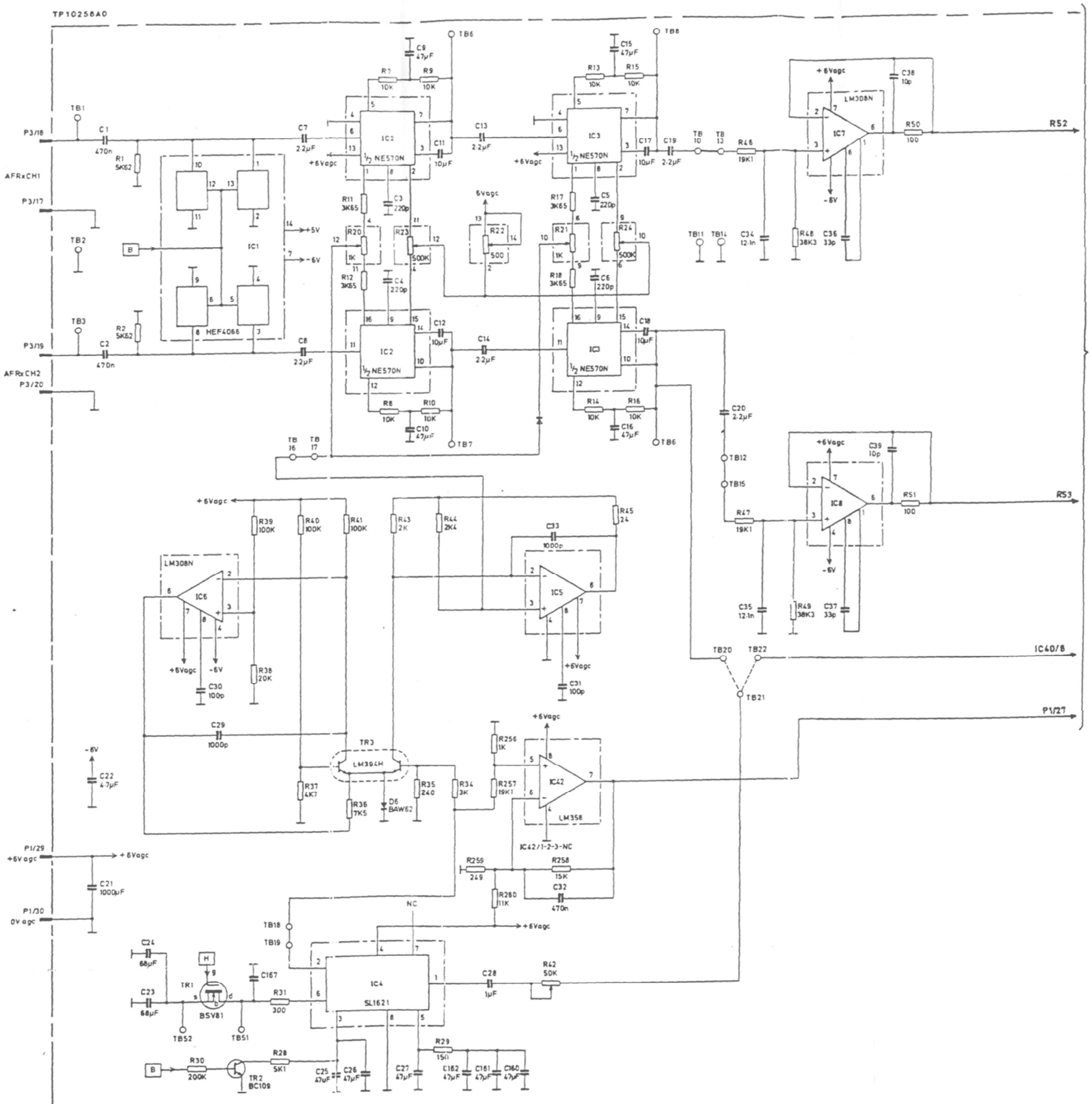


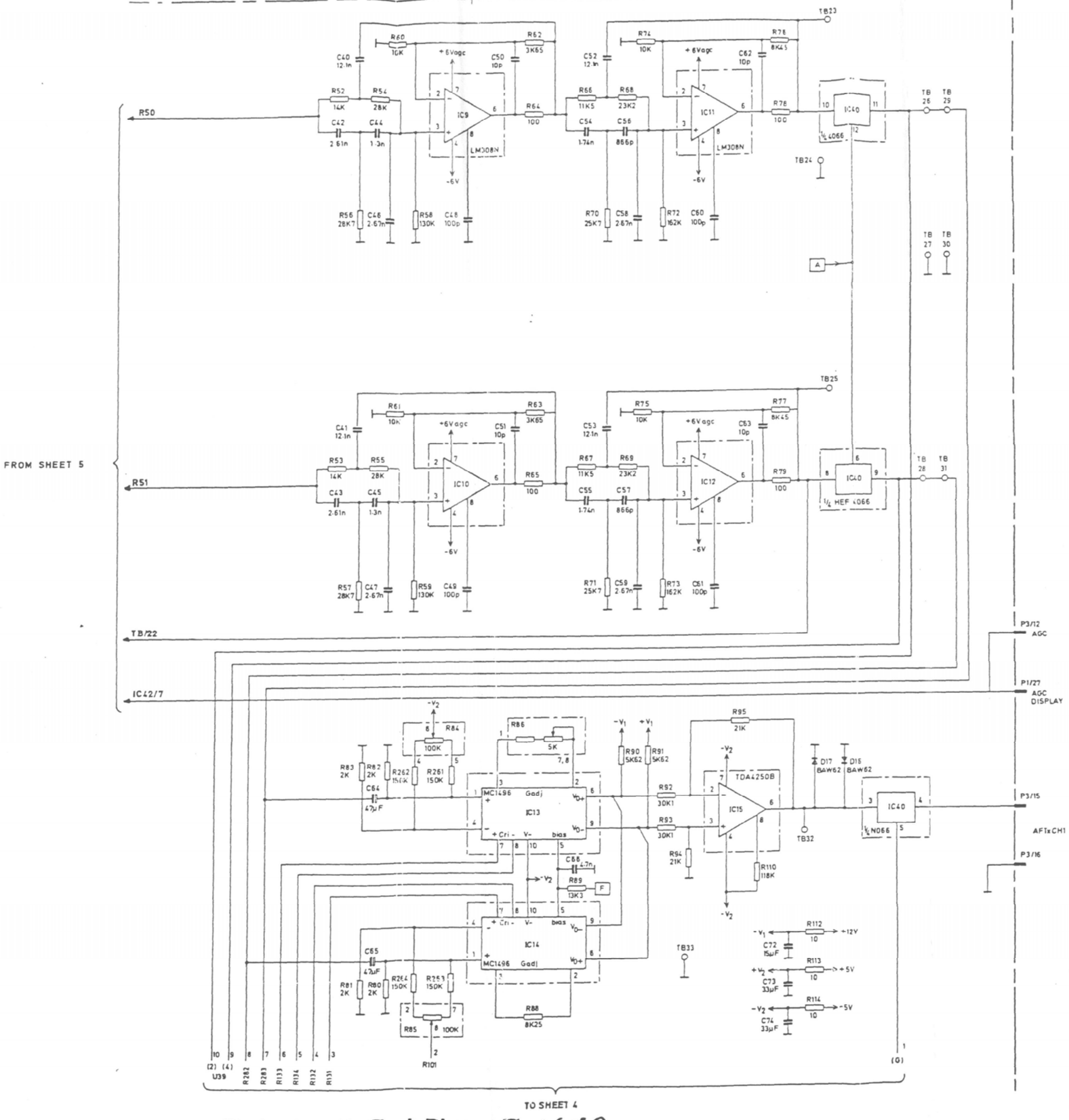
Fig 3.2.3 Phasing Assembly Circuit Diagram (Sheet 4 of 6)



Phasing Assembly Circuit Diagram (Sheet 5 of 6)

Fig 3.2.3

Fig 3.2.3



3.2.3

Phasing Assembly Circuit Diagram (Sheet 6 of 6)

Fig 3.2.3

CHAPTER 3.3

RF HEAD

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CHAPTER 3.3

RF HEAD

INTRODUCTION

1 The RF Head forms part of the Lower Lid Assembly (Fig 3.3.1 - Item 4a) and incorporates one PEC. The following description is to be used with the RF Head circuit diagram (Fig 3.3.4) and as in Chapter 1 the description is sub-divided into the Receiver, Transmitter and Tx/Rx Switching functions.

RECEIVER

RF Amplifier

2 The received signal from the bandpass filters of the ATU is input to the RF Head on J1, and amplified by the rf amplifier TR4. This amplifier provides a small amount of rf gain and isolation between the power splitter and the rf input. TR4 is connected in common base to provide a low noise, low input impedance circuit, which is necessary because the rf input signal is very low (approximately 15 μV). The input signal is connected to TR4 via R3 and dc blocking capacitor C1 and the output of TR4 is transformer coupled to the power splitter (IC1) by T3. This has +12 V fed to its centre tap via R82 and decoupling capacitors C15 and C5.

3 The dc bias current for TR4 is provided by TR8 and TR12 which are switched on by the Tx/Rx switching. This bias can be adjusted by a 1k variable resistor R19, but R19 also supplies a voltage to ZD1 which is used in the AGC network so the bias must be adjusted carefully so as not to affect AGC operation.

AGC Control

4 TR5 is switched on by the Tx/$\overline{\text{Rx1}}$ switching signal via inverting buffer IC5 thus providing a current sink for the diode attenuators D1 and D2. With no AGC voltage applied to J2/12 and with TR5 conducting, D2 is forward biased by the base biasing network of TR4. This means that the incoming received signal sees a low impedance at TR4 emitter.

5 On application of an AGC voltage to its base, TR3 is turned on and the resultant current through D1 and L1 is sunk by TR5. This current increases as the applied AGC voltage is increased, causing a rise in potential at the junction of D1, D2 and L1. This rise in potential reverse biases D2 and the current through D2 falls. If the potential at D2 cathode has risen and the current through it has fallen, this must mean that its impedance has risen. (The inverse is true of D1, whose current has risen, whereby its impedance has fallen.) As D2 is in series with the incoming rf signal, it follows that the signal applied to TR4 is attenuated as the impedance of D2 increases. Thus the AGC voltage effectively controls the amplitude of the output signal. The diode attenuator D1/D2 is decoupled by L1 and C9.

Power Splitter

6 The amplified received rf signal is transformer-coupled by T3 to IC1, which is a power splitter containing a hybrid transformer that splits the rf signal into a pair of identical output signals, ie identical in phase and amplitude. These two signals are fed along two identical signal

paths that have exactly the same functions and circuitry, the only difference being the numbering of the components. To avoid confusion the following text (from here to the end of paragraph 9) will explain the circuit for only one signal path, this text can be used to describe the other signal path by changing the component numbers. D11 and D12 provide over-signal protection for the demodulators, such that if the Rx input signal is high D11 and D12 conduct and short circuit this signal to earth.

Demodulator

7 IC4 is a balanced demodulator that incorporates a diode bridge network, which has applied to it the incoming rf signal and the demodulating signal derived from the Synthesiser frequency by a high speed divider, IC3. The Synthesiser output frequency is fed into the RF Head on P3 and is coupled to IC3, pin 9 via dc blocking capacitor C21. The demodulating signal produced by this divide-by-four IC is fed to IC4 pins 1 and 5 and is 90° out of phase (ie in phase quadrature with the demodulating signal for the other signal path (IC2 pins 1 and 5)). The folded-over spectrum and image frequencies produced by the demodulator are then fed to the low pass filter network, via IC4 pins 3 and 7.

Low Pass Filter Network

8 The lower pass filter network of L10 to L13 and C31 to C35 has a cut-off frequency of 1500 Hz, so only the folded-over audio signal is fed to the low noise amplifier whilst the image frequencies are rejected.

Low Noise Amplifier

9 After filtering, the folded-over audio signal is fed to the low noise amplifier circuit of IC11, IC12, IC13, IC14 and IC16, via TB20/21 and R69. IC11, IC12, IC13, IC14 are 4 ICs that each contain a matched pair of transistors. The transistors are matched so that dc offset voltage is present at their collectors (which are connected in a differential mode), and adjustment for dc 'null' can be made by variable resistor R63. The ICs are all connected in parallel to reduce the source resistance of the differential input to IC16, thereby reducing the level of noise. The differential outputs of the ICs are fed to operational amplifier IC16 via R54 and R55. C39 prevents the amplification of rf signals by IC16. C43 and C48 also prevent rf amplification because as the frequency increases their resistance falls, hence the gain of this stage at rf frequencies is far less than at af when the gain is 1,000, ie the ratio of feedback resistor R68 to input resistor R69. After amplification the folded-over audio signal is fed to Phasing via R65 and the output pin J2/19, along the af Rx CH2 line.

TRANSMITTER

10 The two channels of audio signals are fed to the RF Head from Phasing via the af Tx CH1 and af Tx CH2 inputs, J2/15 and J2/14 respectively. As in receive both channels up to the combiner have identical components and circuitry, excepting that af Tx CH2 is used to generate a cw signal when cw mode is required, for this reason the following circuit description is of af Tx CH2.

Input Amplifier

11 The audio input signal, containing the folded-over spectrum, is fed to the input amplifier, IC18, via J2/14, dc blocking capacitor C51 and input resistor R80. This IC is an operational amplifier and has a gain of approximately 2.

$$\text{gain} = \frac{R71}{R80}$$

It is important for ssb operation that there is no dc component present at the output of IC18, adjustment for 'null' is made by variable resistor R73. From the output of IC18 (pin 6) the amplified signal is fed to the modulator via the low pass filter network.

12 **DC Mode.** In cw mode there are no audio signals present on either of the two af input channels, therefore to generate an rf carrier wave; Channelisation puts the DC Mod input line J2/9 to a logic '1' (+5 V). This dc voltage is fed to pin 3 of IC18 via R79, D15, R90 and the input non-inverting logic IC (IC5 pins 12 and 11). This puts approximately 0.3 V onto pin 3, making the output (IC18 pin 6) 0.6 V. The bridge diodes on IC4 are therefore forward biased and the rf modulating signal is transferred to the output of IC4 (pin 8). This carrier is then fed to the combiner IC1 and, as there is no signal from the other channel, the combined output is a cw signal, which is then processed in the same way as an ssb signal.

Low Pass Filter Network

13 The amplified audio signals from the input amplifier are fed to the modulator, via the low pass filter network which has the same function on Tx as in Rx but in reverse. (See para 8).

Modulator

14 As in receive the output of the Synthesiser is fed via P3 to IC3, which produces two rf modulating signals in phase quadrature. These are fed to the modulator, whose output is therefore an envelope of frequencies containing both upper sideband (usb) and lower sideband (lsb) signals.

Combiner

15 The two signals from both modulators IC2 and IC4, are fed to the combiner IC1 on pins 6 and 5 respectively. IC1 then combines the two phase-related signals to produce a ssb signal, which can be either usb or lsb, depending upon the phase-shifts applied in the audio modulator stage in Phasing.

RF Amplifier and ALC Control

16 The rf amplifier circuit comprising TR6 and TR7 and all associated circuitry, is connected in push-pull, the input and output signals being transformer coupled by T3 and T1 respectively. DC bias for the stage is supplied to TR6 and TR7 bases by TR1 and TR2, via the junction of base bias resistors R16, R17. The bias is applied when the Tx/$\overline{\text{Rx2}}$ input on J2/10 is at a logic '1', which turns TR1 on, via R5 and IC6 pins 6 and 7. Once TR1 is switched on, a collector

current flows via R1 and R2 and turns TR2 on. Thus a dc bias current is applied to the bases of TR6 and TR7, via R16 and R17.

The combined ssb signal is fed to the bases of the push-pull transistors (TR6 and TR7) via T3 terminals 6 and 7, diode attenuators D7 and D8 and dc blocking capacitors C17 and C19. The collectors of TR6 and TR7 are connected to the +12 V supply via the centre-tap of the output transformer T1, which has its secondary connected to the output pin J1 by R3. Frequency compensation for the output transistors is provided by C7, C8 and R8 to increase the gain at high frequencies, whilst resistors R6 and R7, connected between TR6 and TR7 emitters respectively and ground, increase the input impedance of the two transistors.

ALC Control

17 The gain of the rf amplifier is governed by the ALC control circuits, which provide varying levels of bias to the diode attenuators (D7 and D8) connected in series with the signal path, and also to the shunt diode attenuators (D17 and D18). Consequently the level of signal fed to TR6 and TR7 is adjusted, thereby controlling the amplitude of the output signal.

18 As stated in para 16, +5 V is fed to the junction of R5 and R9 when the Tx/$\overline{\text{Rx2}}$ input is at a logic '1', which turns TR9 and TR11 on. Once switched on TR11 provides a constant current sink for the long-tailed pair TR9 and TR10. Thermal compensation for TR11 is provided by D6, which adjusts the base bias of TR11 according to any change in temperature, so keeping the current constant.

19 With no voltage present on the ALC1 input at P2/3, only one half of the long-tailed pair is on, ie TR9, to draw current from the 12 V supply at T3 centre tap. The current path is through T3 to D7/R83 and D8/R84, thus biasing D7 and D8 on.

20 On application of an ALC controlling voltage to the ALC1 input, P2/3, TR10 switches on, drawing its collector current from the +12 V supply via T3 and D18/R85, D17/R86, thus biasing D18 and D17 on.

21 When TR10 is turned on harder by an increase in the ALC controlling voltage, its current increases and, since TR1 is a constant current sink, the current through TR9 must decrease accordingly. Therefore the attenuating diodes D7 and D8, in the serial signal paths to the bases of TR6 and TR7, draw less current, thus their effective impedance increases. Also as the current through TR10 increases, the impedance of 'shunt' diode attenuators D17 and D18 decreases. Hence the signal applied to TR6 and TR7 is reduced, therefore the output level falls. Conversely when the ALC1 voltage falls the output from the RF Head increases.

TX/RX SWITCHING

22 There are two Tx/Rx logic inputs applied to the RF Head by Channelisation for Tx/Rx Switching:

(a) Tx/$\overline{\text{Rx1}}$ - input on J2/8 and P/2/8

(b) Tx/$\overline{\text{Rx2}}$ - input on J2/10

Because some of the receive and transmit signal paths are common, two switching signals have to be used and these make sure that the receiver circuits are switched off before the transmitter

circuits are switched on when going into Tx mode. When switching from transmit to receive the transmit circuits are switched off before the receiver circuits are switched on.

23 Tx/$\overline{\text{Rx1}}$ and Tx/$\overline{\text{Rx2}}$ logic levels are controlled by Channelisation, which puts a logic '0' on both these lines for Rx and a logic '1' for Tx operation. Channelisation also sets the 'timing' of these logic inputs; such that the Tx/$\overline{\text{Rx1}}$ input has a logic '1' put onto it (signifying Tx mode) before a logic '1' is applied to Tx/$\overline{\text{Rx2}}$ and vice versa a logic '0' (for Rx mode) is put on the Tx/$\overline{\text{Rx2}}$ input before the logic on Tx/$\overline{\text{Rx1}}$ is changed.

24 Following the procedure as outlined in paragraph 23 it can be seen that in Transmit mode the logic '1' on the Tx/$\overline{\text{Rx1}}$ input will turn off the receiver circuits, via IC5, before the logic '1' on the Tx/Rx input turns on the transmitter circuits, via IC6. Conversely in Receive mode the logic '0' on Tx/$\overline{\text{Rx2}}$ turns off the transmitter circuit before the logic '0', applied a little later to the Tx/$\overline{\text{Rx1}}$ input turns on the receiver circuits.

INTERCONNECTIONS

25 The RF Head provides through routing for two signals that have no circuit connection to the RF Head components. These two signals are:

(a) Low/High Power from J2/7 to P2/9

(b) Tx Protect from J2/5 to P2/7

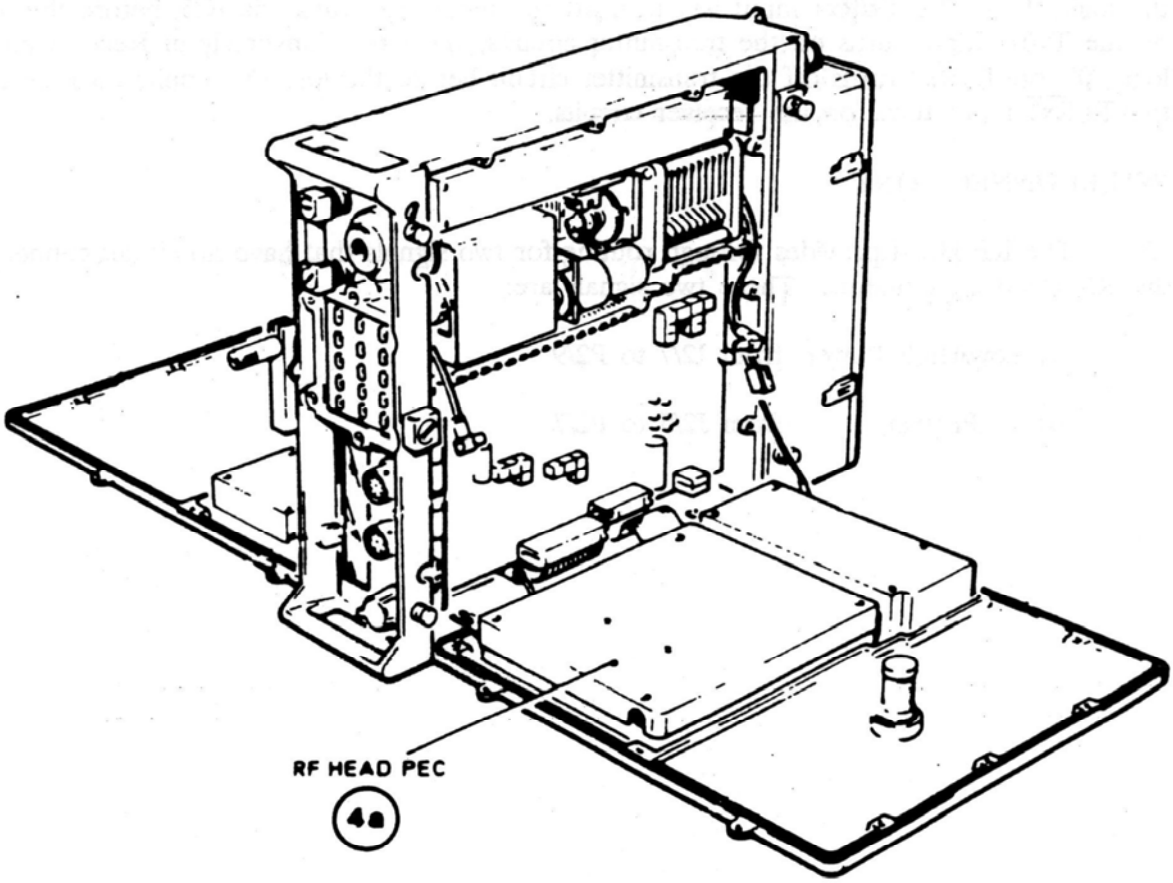


Fig 3.3.1 RF Head PEC Location

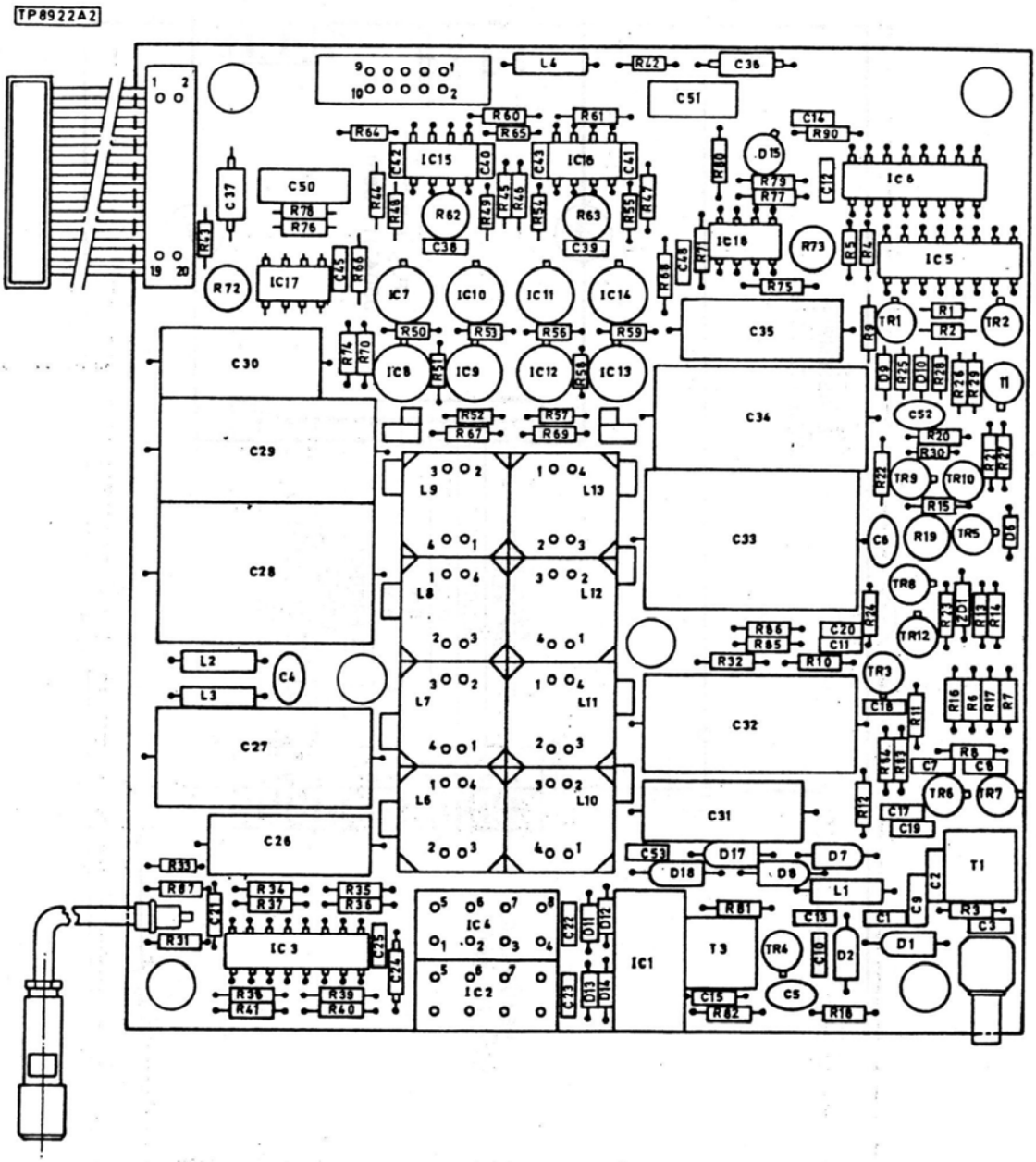
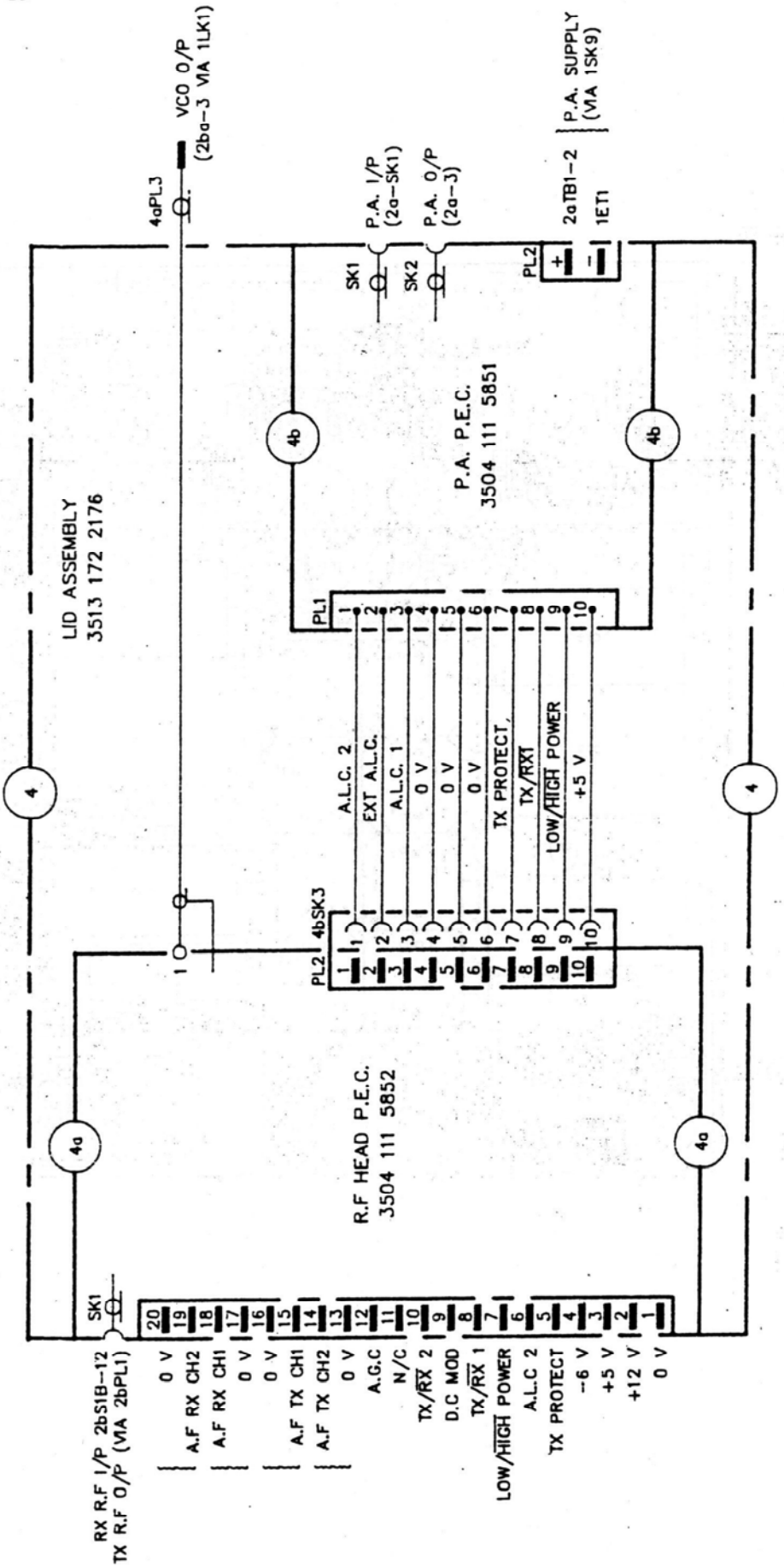
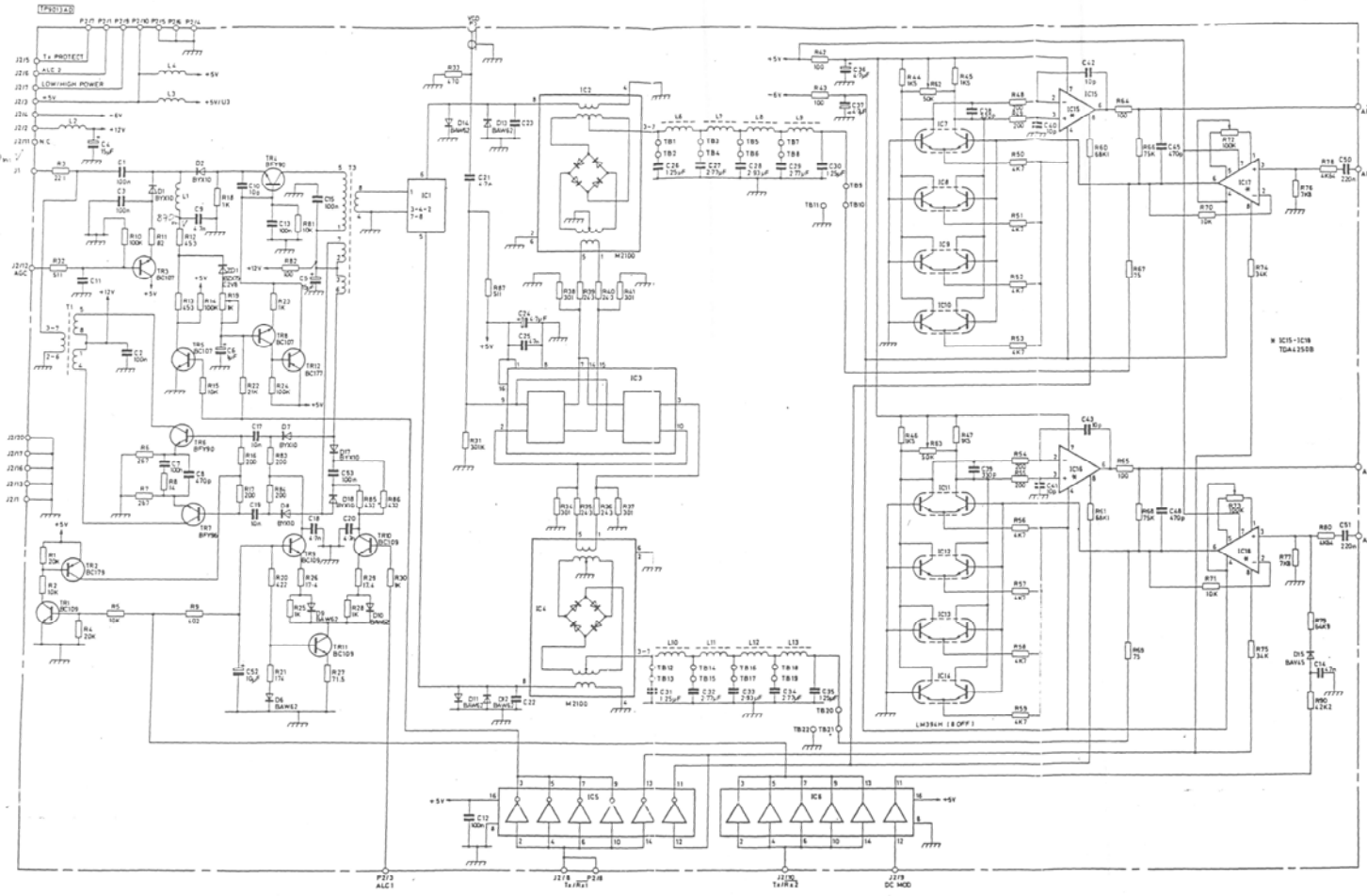


Fig 3.3.2 RF Head PEC Component Location



TP10311C

Fig 3.3.3 PA/RF Head Lid Assembly Interconnection Diagram



g 3.3.4

RF Head Circuit Diagram

Fig 3.3.4

CHAPTER 3.4

SYNTHESISER

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CHAPTER 3.4

SYNTHESISER

INTRODUCTION

1 The Synthesiser, forms part of the Upper Lid Assembly (Fig 3.4.1 - Item 3b) and it consists of two PECs containing all of the Synthesiser circuits (Fig 3.4.2/3). ICs on Synthesiser 1 (VCO) PEC have no prefix, while those on Synthesiser 2 (Auto-null) PEC have the prefix B.

CIRCUIT DESCRIPTION (Fig 3.4.4)

Reference Oscillator

2 The reference oscillator, IC10, is a crystal-controlled temperature compensated oscillator, having an output frequency of 5.12 MHz. Initial setting and ageing compensation is provided by R14.

Frequency Divider

3 The 5.12 MHz reference frequency is applied to the B input of frequency divider IC11 where it is divided by five to give a 1.024 MHz square wave at the QD output, pin 11. This signal is used as a clock for the microprocessor contained on Channelisation and is fed to this PEC via PL1/2. The 1.024 MHz clock is also connected to the A input of IC11 and is further divided by a factor of 2, producing a 512 kHz square wave at the QA output, pin 12.

4 The 512 kHz square wave present at IC11/12 is then fed to the frequency synthesiser IC, (IC12), to be divided-down to the comparison frequency rate of 4 kHz. The frequency synthesiser IC also contains the phase comparator and phase modulator. See Figure 3.4.5 for an internal functional block diagram of IC12.

5 The use of external crystal reference oscillator (IC10) means that the internal crystal oscillator of the frequency synthesiser IC (IC12), is not required. Therefore, the internal reference oscillator is biased externally by R16 to operate as a buffer amplifier. The 512 kHz reference signal is ac coupled to pin 22 of IC12 by C4. IC12 contains two dividers in series, which are both programmable. The division ratio of each of the dividers is governed by the programming logic, which in turn is set by externally connected voltages.

6 The prescaler within IC12 has selectable division ratios of 1, 2, 10 or 100, according to the voltage levels on NS_0 and NS_1 (pins 23 and 24). NS_0 is connected to +10 V, whilst NS_1 is grounded so the prescaler is set to divide by 2. (See Table 3.4.1.)

7 The divider is a binary divider with a programmable division ratio of 1 to 1024. The division ratio is set up by the binary number on pins A_0 to A_9. Pin 17, A_6, is connected to +10 V, whilst A_0 to A_5 and A_7 to A_9 are all connected to the 0 V rail. This gives a division ratio of $2^6 = 64$. Therefore, the overall division ratio of the two dividers is $2 \times 64 = 128$, thus providing the circuit with a 4 kHz reference comparison frequency. This signal is fed out of IC12 via pin 26 (OUT). A link is made on the PEC between IC12/26 and IC12/25, which connects

the reference comparison frequency to the phase comparators. Another connection is also made at this point which provides a programme clock for the universal divider (UD), IC9 pin 13. (See Programmable Divider, paras 20 to 31.)

Table 3.4.1 Selection of Prescaler Division Ratio

NS_0	NS_1	Prescaler Division Ratio
0	0 V	1
+10 V	0 V	2
0 V	+10 V	10
+10 V	+10 V	100

DATA STORE

8 The data store consists of three shift registers, (IC1, IC2 and B/IC3), three inverting buffers (IC4, IC5 and IC6) and a <10 MHz decoder (B/IC1 on sheet 2). The Data Input to the shift registers is produced by Channelisation, whenever there is a frequency change, and is fed to PL1 pin 7 of the Synthesiser. This data is generated in serial form and is fed into IC1 pin 2 as a 24-Bit data stream. Channelisation actually generates 2 x 12 Bits of data. The first 12 bits of data contain the VCO Band, 10 MHz, 1MHz and 100 kHz codes in 2 x 2-bit words and 2 x 4-bit words. The second 12 bits of data contain the 10 kHz, 1 kHz and 100 Hz codes in 3 x 4-bit words (see Table 3.4.2).

9 The 24-bit serialised data is loaded into the three cascaded shift and store registers (IC1, IC2 and IC3) by the Data Clock pulses fed to the Synthesiser from Channnelisation. These clock pulses are then fed to pin 3 of IC1, IC2 and IC3 via PL1/9. The serial output of IC1, ie pin 9, is connected directly to the data input of IC2 and likewise IC2 is cascaded to IC3. Therefore, on the positive edges of the data clock serial data is shifted until the registers are loaded.

10 After the 24th clock pulse, Channelisation produces a 1 µsecond Strobe pulse. This is fed to the STR input of each shift and store register, ie IC1, IC2 and IC3 pin 1. The output enable, E_0, of each shift and store register, is connected to +10 V, therefore on the application of a Strobe pulse the data in the shift registers is transferred to the output as well as into the storage register of each IC.

Note: The data now present in the storage registers and on the outputs of IC1, IC2 and IC3 is retained and remains stable. When a frequency change takes place, a new 24-Bit Data Stream is produced and the whole process starts again.

11 The frequency and VCO band code information is now in parallel form. All of this data is fed to three inverting buffers, except for the VCO band code and the 100s Hz code. The VCO band code present on IC3 pins 11 and 12 is connected to IC15c and IC15d (see VCO, paras 14 to 19). The 100s of Hz data on IC1 pins 4, 5, 6 and 7 is fed to IC13 pins 15, 1, 3 and 5 (see Rate Selector, and Phase Jitter Predict, paras 32 to 37).

12 The remaining data (ie 10s of MHz, 1s of MHz, 100s of kHz, 10s of kHz and 1s of kHz) present at the outputs of the shift and store registers, is fed to three inverting buffers, IC4, IC5 and IC6. These buffers are used to store the frequency data until they are addressed by the UD (IC9). When these buffers are addressed, the data that they hold is inverted and is used to programme the division ratio of the UD (IC9), (see Programmable Divider, paras 20 to 31).

Table 3.4.2 24 Bit Data Stream Contents

Encoded Data	100s of Hz				1s of kHz				10s of kHz				100s of kHz				1s of MHz				10s of MHz		VCO Band	
Type of Code	4-bit BCD				4-bit BCD				4-bit BCD				4-bit BCD				4-bit BCD				2-bit Binary		2-bit Binary	
Circuit Ref	D	C	B	A	D	C	B	A	D	C	B	A	D	C	B	A	D	C	B	A	B	A	B	A
Bit Number	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Example - 20 MHz	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	H
Example - 12.6 MHz	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L	L	L	H	L	L	H	H	L

Note: H - HIGH - +5 V
L - LOW - 0 V

13 The 10s of MHz data on IC3 pins 13 and 14 is also connected to a < 10 MHz decoder and the Auto-null circuit, via PL3 pins 6 and 5. Referring to Fig 3.4.4 Sheet 2, the Auto-null circuit consists of B/IC2 to B/IC9 and their associated components. (See Auto-null circuit Paras 61 to 67). B/IC1, on Sheet 2, is the <10 MHz decoder, which has two address inputs (AOA and AIA) an active low enable $\overline{EA}$ and an active low output ($\overline{O}$OA). The 10s of MHz data is fed to the address inputs and the output at B/IC1 pin 4 will always be high unless both address inputs and the enable input are all low. The enable input B/IC1 is connected to IC9 pins 5, 16 and 17, via PL3 pin 14 and the output of B/IC1 is connected to IC9 pins 18 and 19 via PL3 pin 13 (see Programmable Divider, paras 23 to 31).

VOLTAGE CONTROLLED OSCILLATOR (VCO)

14 The voltage controlled oscillator contains two switchable Hartley oscillators, one having an oscillatory range of 12.8 to 36 MHz and the other having a range of 60 to 120 MHz. These ranges of oscillatory frequencies are either put through a high speed divider (IC18) or fed through a diode gate (D11) that bypasses the divider. The total range of VCO frequencies, divided and undivided, provides a synthesiser output frequency range of 6.4 to 120 MHz. Switching of the two oscillators and selection of the divider/diode gate is enabled by the VCO band code data present at IC3 pins 11 and 12 (see Data Store, paras 8 to 13).

15 When either TR7/1 or TR7/2 is switched on by the band code bit from IC3 pin 11, it provides a constant current source for its related FET whose circuit then oscillates. When IC3 pin 11 is at a logic '0', TR7/1 is off and TR7/2 is turned on (via the inverting buffer IC15/3 pin 10), therefore TR8 oscillates. Conversely, when IC3 pin 11 is at a logic '1' (+5 V), TR6 oscillates. The oscillatory signals are then fed to the divider/diode gate, via C29.

16 When IC3 pin 12 is at a logic '0', TR11 turns on and supplies the high speed divider (IC18) with +6 V VCC. So any signals present on IC18 input pin 1 are divided by 2 and fed out on IC18 pin 7. Conversely, when IC3 pin 12 is at a logic '1' (+5 V), TR9 will be turned on via IC15d pin 12 and a biasing voltage of +6 V forward biases D11. Therefore, any signal present at D11, C33, C29 junction, bypasses the divider (see Table 3.4.3).

17 All oscillatory signals, from IC18 pin 7 or D11 cathode, are fed to TR2 via LK3. TR2/TR3 and associated circuitry is a buffer amplifier circuit to match the input impedance of the prescaler IC8. The oscillator output is then divided down to the comparison frequency of 4 kHz by IC8 and IC9. All oscillatory signals are also fed to TR12 base via dc blocking capacitor C43. TR12 is connected in emitter-follower configuration and is used as a buffer/impedance matching transistor to match the impedance of the quadrature dividers contained on the RF Head. The oscillatory signals present at TR12 are therefore fed to the RF Head as a Synthesiser output signal, via C49 and PL2.

18 A stable +10 V dc supply for the VCO is obtained from the +12 V input on PL1 pin 10. The +12 V supply is fed to TR4 via rf choke L8. TR4 is connected as a voltage follower and its emitter is at +10 V. RF decoupling for this stabiliser is performed by C22 and C24.

19 Voltage control of both VCOs is performed by the controlling voltage produced at IC19 pin 6. This voltage is fed to varactor diodes D6, D7, D8 and D9 (contained within the tank circuit of each oscillator) via LK5. For a Hartley type oscillator:

$$fosc = \frac{1}{2\pi\sqrt{LC}}$$

Therefore, if the value of C is increased, the oscillatory frequency will decrease. Thus a decrease in controlling voltage applied to the varactor diodes will increase the effective capacitance leading to a decrease in VCO frequency. Typically, the range of controlling voltage applied to the varactor diodes is from 2 to 9 V. As a general rule, the lower the frequency within each band, the lower the controlling voltage applied. Conversely, the higher the oscillatory frequency in each band, the higher the controlling voltage applied to attain that frequency. For example, VCO Band 2 selection is equivalent to a dialled frequency ranging from 4.5 to 7.999 MHz. When 4.5 MHz is selected as the operating frequency, then the controlling voltage applied to the varactor diodes is approximately 2.5 V. Whereas when 7.999 MHz is selected as the operating frequency, the controlling voltage is approximately 8.5 V.

Table 3.4.3 VCO Band Selection

VCO BAND	DIALLED FREQUENCY RANGE (MHz)	SYNTHESISER OUTPUT FREQUENCY RANGE (MHz)	VCO BAND CODE A	VCO BAND CODE B	TR8/TR6 SELECT	IC18/D11 SELECT
1	1.6 to 4.49	6.4 to 17.999	0	0	TR8	IC18
2	4.5 to 7.99	18.0 to 31.999	1	0	TR8	D11
3	8.0 to 14.99	32.0 to 59.999	0	1	TR6	IC18
4	15.0 to 30.000	60.0 to 120.000	1	1	TR6	D11

PROGRAMMABLE DIVIDER (Figs 3.4.6, 3.4.7 and 3.4.8)

20 The purpose of the programmable divider is to divide down the VCO frequency to the comparison frequency of 4 kHz. Any change in the overall division ratio of the programmable divider leads to a change in the Synthesiser output frequency. Most of the circuitry of the programmable divider is contained in the UD (IC9). The maximum input frequency that IC9 can operate with is approximately 15 MHz. The VCO output frequency ranges from 6.4 to 120 MHz so a 'prescaler' is needed to divide the VCO frequency prior to its being fed to the UD.

Prescaler (Fig 3.4.6)

21 IC8 is a dual modulus prescaler that can be logically programmed to divide by either 10 or 11. The CK input, pin 1, is ac coupled to the VCO output buffer transistor TR3. R4 prevents the divider self-oscillating when there is no input signal present. The division ratio is controlled by inputs, PE1 and PE2. IC8 divides by ten when either input is high and by eleven when both inputs are low. The controlling logic signals on IC8 pins 2 and 3 are generated by IC9, which produces two trains of pulses on the $\overline{\text{OFB1}}$ and $\overline{\text{OSY}}$ pins. IC9 pin 22 ($\overline{\text{OFB1}}$) and IC9 pin 21 ($\overline{\text{OSY}}$) are connected to PE2 and PE1 respectively, via two blocking diodes D3 and D4. These prevent the +10 V that is present on $\overline{\text{OSY}}$ and $\overline{\text{OFB1}}$, when these pins are high, from damaging IC8.

22 The divided-down VCO frequency is fed from IC8 pin 11 to IC9 pin 20. IC8 pin 11 is interfaced to drive the CMOS logic of IC9 by R13. Figure 3.4.6 shows the relationships of the divided output and the two controlling logic inputs (PE1 and PE2). The purpose of the OSY signal is to synchronise the PE1 input to the prescaler. $\overline{OSY}$ goes low every time the UD produces an output at OFS. As the OFS output is at 4 kHz the $\overline{OSY}$ pin goes low every 250 µseconds. The duration of the low is dependent upon the frequency out of IC8, ie the low on $\overline{OSY}$ has the same pulse duration as the frequency on pin 20 (IN). $\overline{OFB1}$ goes low when the prescaler is instructed to divide by 11 and the signal stays low for 250 µseconds, ie for one basic timing period of the OFS output. When $\overline{OSY}$ or $\overline{OFB1}$ go low the voltage levels on PE1 or PE2 fall from +VCC to approx 2.75 V, via resistors R5, R6, R1 and R12.

Universal Divider (Fig 3.4.7 and 3.4.8)

23 The UD (IC9), together with its prescaler (IC8), make up a fully programmable divider with 6 decades of control. The total division ratio is dependent upon the frequency data loaded into the A and B inputs and the $\overline{RI}$ command input.

24 A block diagram of the internal configuration of IC9 is shown in Figure 3.4.7. The programming of the UD is timed and controlled by inputs PC and PE. When the programme enable (PE) input is high, the positive edges of the programme clock (PC) signal step through the internal programme counter in a sequence of 8 states. Seven of the states define fetch periods, each indicated by a low signal at one of the corresponding data address outputs ($\overline{OD0}$ to $\overline{OD6}$). These data address signals are used to address the external programme source held in the inverting buffers (IC4, IC5, IC6) and the <10 MHz decoder (B/IC1, Sheet 2). The data fetched from the external programme source is applied to inputs $\overline{A0}$ to $\overline{A3}$ and $\overline{B0}$ to $\overline{B3}$. When PC is low, in a fetch period, an internal load pulse is generated and any data present in the data decoder is decoded and used to programme the division ratio of the internal dividers. Timing of PC, PE, output addresses $\overline{OD0}$ to $\overline{OD6}$ and internal load pulses is shown in Figure 3.4.8.

25 The programme clock, PC, is connected to the R and OUT pins of IC12 which have the comparison frequency signal of 4 kHz present on them (see frequency divider, para 7). Therefore PC is always running and is at a frequency of 4 kHz. The programme enable, PE, input is provided by the D type flip-flop, IC7b. PE is low until IC7b has a positive signal fed to its input, pin 8, which is connected to the STROBE input PL1 pin 5. At the end of the 24-bit data stream, a strobe pulse is generated by Channelisation. This positive pulse sets IC7b and its output goes high. Therefore, PE goes high and on the next positive transition of PC the programme counter in the UD puts $\overline{OD6}$ high, which is a start state.

26 On the next positive transition of PC, $\overline{OD0}$ goes low. This low on $\overline{OD0}$ is fed to the active low enable pin of IC4. Therefore, the 1s of kHz data present at IC4 pins 2, 4, 6 and 10, is inverted and applied to the data A inputs of IC9 $\overline{A0}$-$\overline{A3}$. On the next negative going edge of PC an internal load pulse is generated and the data applied to $\overline{A0}$-$\overline{A3}$ is processed in the internal data decoder. The data decoder then produces programming information that programmes the dividers in the UD.

27 The next positive transition of PC puts $\overline{OD0}$ high and $\overline{OD1}$ low. $\overline{OD1}$ is connected to pin 15 of IC4 and IC5, thus the 10s of kHz data present on the inputs to these buffers is inverted and applied to $\overline{A0}$-$\overline{A3}$ inputs of IC9. Yet again, the negative transition of PC results in an internal load pulse and the data on $\overline{A0}$-$\overline{A3}$ is used to programme the dividers in the UD. The process continues through $\overline{OD2}$, $\overline{OD3}$ and $\overline{OD4}$. When $\overline{OD4}$ is put low the 10s of MHz data on IC6 pins 12 and 14 is inverted and applied to the $\overline{A1}$ and $\overline{A0}$ data input respectively.

The other two data inputs, $\overline{A2}$ and $\overline{A3}$, will be at +10 V via R7, R8, R9 and R10 in the absence of a data 'low'.

28 On the next positive transition of PC, $\overline{OD5}$ goes low and no new data is accepted or presented. $\overline{OD5}$ stays low for one clock period of PC, 250 µsecs then goes high. $\overline{OD5}$ is connected to the CP input of IC7b, thus when $\overline{OD5}$ goes positive IC7b is reset. The output pin of IC7b then assumes the logic level on pin 9, which is held low by being connected to 0 V. Therefore, PE goes low and stays low until a Strobe pulse sets IC7b. The low on the PE input to the UD puts $\overline{OD6}$ low on the next positive PC transition.

29 The low on $\overline{OD6}$ puts a low on $\overline{A1}$ and $\overline{A3}$ via diodes D1 and D2. The other two inputs $\overline{A0}$ and $\overline{A2}$ are high via pull-up resistors R7 and R9. $\overline{OD6}$ is also connected to inputs $\overline{B0}$ and $\overline{B1}$ which are therefore low. $\overline{B0}$ and $\overline{B1}$ are connected to the active low enable of the <10 MHz decoder B/IC1 via PL3 pin 14, (see Data Store, para 13). IC1 pin 4 is connected to the other two inputs $\overline{B2}$ and $\overline{B3}$, via PL3 pin 13. When the frequency is 10 MHz or above, then $\overline{B2}$ and $\overline{B3}$ are high, conversely when the frequency is below 10 MHz, $\overline{B2}$ and $\overline{B3}$ are low. On the next negative transition of PC, an internal load pulse is generated and the A and B inputs are processed in the internal data decoder. The data decoder then produces programming information that is used to programme the dividers of IC9.

30 The internal dividers of the UD consist of a chain of dividers operating in a programmable mode. Control of the external prescaler (IC8), is provided by these dividers, which produce the synchronising signal $\overline{OSY}$, and the modular control signal $\overline{OFB1}$. The divided down VCO frequency from the prescaler (IC8), is fed into IC9 on the IN input, pin 20. The output frequency of 4 kHz from the UD is fed to IC12 pins 1 and 2, for phase comparison with the comparison frequency, via the OFS output pin 25 (see Phase Comparator, para 45). OFS is also connected to:

(a) IC14 pin 9 (see Rate Selector and Phase Jitter Predict, para 34)

(b) IC15b pin 9 (see Auto-null, paras 61 to 67)

31 A low on the $\overline{RI}$ input pin of IC9 permits selection of the 400 Hz synthesised output frequency steps by 'side-stepping' one of the dividers contained in the UD. For generation of the $\overline{RI}$ input pulse see Rate Selector and Phase Jitter Predict, paras 32 and 36.

RATE SELECTOR AND PHASE JITTER PREDICT (Fig 3.4.4)

32 IC13 and IC14 operate together as a successive addition rate multiplier to produce the 'side-step command' and 'phase-jitter predict' signals. When the 100s of Hz data lines at IC1 pins 4-7 are all low, this network is inoperative. It only functions when any or all of the 100s of Hz data lines are high (see Data Store, paras 8 to 13).

33 The 100s of Hz data is fed to IC13, a BCD adder. The least significant data bit ('A' digit) is fed to the A1 input, pin 15, and the most significant data bit ('D' digit) is fed to the A4 input, pin 5. IC13 adds the A1-A4 inputs to the B1-B4 inputs producing sum and carry outputs in BCD code. The sum outputs on S1-S4 are fed to IC14. The carry output on IC13 pin 9 is fed to IC9, pin 26, via the inverting gate of IC15a (see Programmable Divider, para 31). The carry output of IC13 is also 'latched' through IC14 to IC7a pin 5, which is part of the Auto-null circuit.

34 The sum and carry data present on data inputs D0-D4 of IC14 is transferred to the outputs, O0-O4, on positive transition of the clock pulse fed to the clock input, IC14 pin 9. This clock pulse is provided by the OFS output of IC9, pin 25, which is at a frequency of 4 kHz only when the output frequency is correct. The master reset input of IC14, $\overline{MR}$, is connected to +10 V, which enables the clock to transfer data from input to output.

35 Output pins O0-O3 of IC14 are connected to the B inputs of IC13 and the data present on these lines is summed with the data on the A inputs.

36 From the table it can be seen that for 300 Hz selection, 3 carry out pulses are generated in a complete count of 10. The carry out pulse is fed from IC13 pin 9 to IC15a where it is inverted. Thus, a logic '0' is put on the $\overline{R1}$ input to IC9 three times in 10 counts. The count sequence for this successive addition rate amplifier then continues until the radio is switched off or a new frequency is entered that does not contain any 100s of Hz data bits.

37 The data present on IC14 output pins is the same data as that present on IC13 outputs but occurs one clock pulse later. Therefore, the data on IC14 pins O0 to O3 is in proportion to the carry out pulse that is fed to IC9 as a sidestep command. Thus the data on IC14 pins O0 to O3 can be used as a phase-jitter predict signal and as such is fed to IC16.

MOD GENERATOR (Fig 3.4.4)

38 The MOD generator circuit consists of IC16 and IC17a, which produces a MOD signal that is used to cancel the phase-jitter present on the OFS signal of IC9. IC16 is a multiplying digital to analogue converter, which multiplies the dc on Vref by the digital number on data lines D4 to D7. The Vref voltage is fed from the Auto-null circuits (on sheet 2) via PL3 pin 18 and the buffer/gain compensation amplifier of IC17d (see Auto-null, paras 61 to 67). Data lines D0 and D3 are all connected to 5 VA which is the ground reference for IC16. Data lines D4 to D7 have pull-up potential dividers connected to them, thereby referencing a '0' data bit to the same ground reference, ie 5 VA.

39 IC17a is a summing op-amp that produces an output voltage relative to the current at its input, ie IC16 pins 1 and 2. This voltage at pin 1 IC17a, is equal to the digital numbers on D4-D7 inputs multiplied by the dc voltage on Vref of IC16. Vref is negative with respect to 5 VA.

40 The data on D4-D7 is changing at the OFS frequency rate 4 kHz, therefore the waveform produced at IC17/a pin 1 is a sampled ramp. Figure 3.4.9 gives some examples of these waveforms. For low order selection of 100 Hz numbers, the ramp starts at 5 VA and steps up to a more positive potential. For higher order numbers the maximum value of the ramp starts at a more positive potential and steps down to 5 VA. The peak to peak amplitude of the MOD waveform is governed by the Vref voltage generated by the Auto-null circuit. Thus, the peak to peak amplitude is greater at low Synthesiser output frequencies than the amplitude at high Synthesiser output frequencies.

Note: If there is no 100s of Hz selection, IC17a pin 1 will be a continuous dc voltage of +5 VA.

41 The sampled ramp waveform present at IC17a pin 1 is then fed to the phase modulator contained in the frequency synthesiser (IC12), via the MOD input pin.

PHASE MODULATOR (Fig 3.4.5 and 3.4.10)

42 The phase modulator is contained in the internal circuitry of the frequency synthesiser (IC12), which is shown on the block diagram (Figure 3.4.5). By means of a timing circuit the phase modulator produces an internal delay pulse, V^1, which is then fed to the phase comparators. The characteristic of the V^1 pulse is dependent upon the two inputs to the phase modulator. These are the divided-down VCO frequency, (OFS output of IC9) which is fed to the V input of IC12 pin 1, and the signal generated by IC17a which is fed to the MOD input of IC12 pin 27. Any pick-up of rf on the MOD input signal line is decoupled to ground by R83 and C51, thus ensuring that the internal V^1 pulse is not corrupted by unwanted signals.

43 The timing circuit of the phase modulator is enabled by one external capacitor, C8, which is connected to the TCB input. A negative going transition at the V input causes C8 to produce a positive-going linear ramp. When the ramp has reached a value almost equal to the modulation input voltage, at the MOD input, the ramp terminates and C8 discharges. Figure 3.4.10 shows the relationships between the input signals, TCB ramp and the output delay pulse of V^1 when 100 Hz has been selected.

44 When C8 is discharged, the V^1 pulse is at a high value. Once C8 starts to charge, V^1 goes to a low value and remains low until the ramp of C8 is terminated. V^1 then returns to its high value and the cycle repeats. The V^1 pulse is then fed to both phase comparators.

Note: When MOD input signal is constant (as occurs when there is no selection of 100s of Hz decade) the V^1 output pulse width also remains constant.

PHASE COMPARATORS (Figs 3.4.5, 3.4.11, 3.4.12, 3.4.13)

45 The frequency synthesiser (IC12) contains two phase comparators, PC1 and PC2. PC2 produces an error voltage that is used to 'coarse' tune the VCO. Once the VCO frequency has been coarse tuned to within the capture range of PC1, PC2 is disabled and fine control of the VCO is maintained by PC1. Both comparators are shown on Figure 3.4.5, the internal block diagram of IC12.

PC2

46 PC2 functions as a frequency discriminator and compares the V^1 input pulse with the R input. The V^1 pulse is generated by the phase modulator and is at the same frequency as the V input to IC12 (OFS output of IC9). The R input is the comparison frequency of 4 kHz. PC2 output has three states:

(a) When the frequency of V^1 is much greater than the frequency of R, PC2 output goes permanently high.

(b) When the frequency of V^1 is much less than the frequency of R; PC2 output goes permanently low.

(c) When the frequency of V^1 is close to that at the R input.

47 PC2 also produces an out of lock signal (OL goes high) which is always present when PC2 is operative. Thus the out of lock signal is present when:

(a) The frequency of V^1 is much greater than R.

(b) The frequency of V^1 is much less than R.

(c) The R input signal is missing.

(d) The V input to IC12 is missing.

This out of lock indication appears at IC12 pin 4, which is connected to the varicap trigger circuit and PL1 pin 3 (see Loop Filters, paras 54 to 57).

48 When the PC2 output goes open circuit (V^1 is close to R) internal circuitry provides an enable for PC1 and puts the OL output low. Thus the out-of-lock indication is removed and 'fine' control of the VCO is performed by PC1. PC2 output pin (IC12 pin 9) is connected to the loop filter circuit of IC19 via LK1 (see Loop Filter, para 54).

PC1 (Fig 3.4.11, 3.4.12 and 3.4.13)

49 PC1 is a 'sample and hold' type phase comparator which uses external capacitors as timing components (see Figure 3.4.5). C7 is connected to the TCA input, and C9 is connected to the TCC input.

Note: R17 is connected between TRA and the 0 V rail to provide a bias current path to ground for all of the analogue devices of IC12, (phase modulator and phase comparators). This line is rf decoupled by C21.

50 A negative going transition at the V input causes the 'sampling' capacitor C7, to be discharged. After a specified delay, caused by the phase modulator by means of the internally generated V^1 pulse, C7 charges up positively, producing a linear ramp at the TCA input. A negative-going transition at the R input terminates this ramp. The voltage on C7 is now 'sampled' by means of an internal sampling switch, and then transferred to C9 the 'hold' capacitor. The voltage on C9 is in turn buffered and made available at the PC1 output. On the next negative going transition of the V input the sampling capacitor, C7 is discharged and the cycle repeats (see Figure 3.4.11).

51 Consider the case when there is no selection of 100s of Hz. The divided-down VCO frequency (OFS of IC9) fed to the STB input, discharges C7, on the negative going edge, then after a very small delay, caused by the V^1 pulse, C7 ramps up. Very soon after this the negative-going edge of the R input (R input = comparison frequency) terminates the ramp. The voltage on C7 is thus transferred to PC1 output via C9. On the next transition of the OFS output of IC9, C7 is discharged and the cycle repeats. Thus PC1 output voltage remains at a constant amplitude.

52 Figure 3.4.12 is a diagrammatical representation of PC1 waveforms when there is 100s of Hz selection but no signal on the MOD input:

(a) Figure 3.4.12(a) shows the comparison frequency input to PC1 on the R input pin.

(b) Figure 3.4.12(b) is the divided-down VCO frequency applied to the V input, IC12 pin 1.

(c) Figure 3.4.12(c) is the internally generated V^1 input to PC1. This is generated by the phase modulator, which, in this instance, does not have a signal on the MOD input applied to it. Thus the V^1 pulse width stays constant.

(d) Figure 3.4.12(d) is the ramp waveform appearing on C7 (TCA pin).

(e) Figure 3.4.12(e) is the resultant PC1 output waveform, which in this instance causes frequency and phase modulation of the VCO output.

53 Now consider the normal operation of PC1, where 100 Hz has been selected and a varying signal at the MOD input is applied to the phase moduator. Figure 3.4.13 is a theoretical representation of the resultant waveforms of PC1. The R input pulse is obtained from the internal reference oscillator and therefore stays constant. V input varies because of the phase-jitter introduced. In this instance, the V^1 pulse (generated by the phase modulator) varies in width, but the time interval between its positive going edge and the negative transition of the R input remains constant. Therefore the TCA ramp reaches the same amplitude at each sample point. This results in a steady voltage at the PC1 output, thus the controlling voltage fed to the VCO via the loop filter is clear of any 'ripple' that could have been caused by phase-jitter.

LOOP FILTER

54 The loop filter consists of IC19 and its associated circuitry. IC19 is an operational amplifier (op amp) with the non-inverting input connected to a +6 reference. With PC1 and PC2 connected to the invert input pin 2, IC19 produces a ramp between about 1 V and 9 V from the positive-going and negative-going pulses of the PC2 output. The gap in the characteristic of PC2 in which only PC1 operates provides the high loop locking speed of the filter.

55 The dc gain of IC19 is very high, but the ac gain is limited by the values of C39, C41, R74 and R73. Thus any ac component of PC1 or PC2 output is filtered out. R71 is a much smaller value than R69 to enable PC2 quickly to coarse tune the VCO (ie to attain VCO lock). Both phase comparators increase their output voltages as the signal from the UD, V, leads the input from the reference divider, R. IC19 inverts the PC1/PC2 outputs, to effect a decrease in control voltage to the VCO. Thus the VCO output frequency also decreases resulting in effective control of the loop.

56 Under PC1 control a small change in PC1 voltage results in a large change in IC19 output voltage. For stability of the loop, the reference voltage applied to IC19 pin 3 is both audio and rf decoupled. The VCO controlling voltage supplied by IC19 is connected to varicap diodes in both tank circuits of the VCO via isolating resistors R52/62 and LK5.

57 Very low varicap control voltages can occur when the VCO is out of lock, ie when PC2 is being used to control the loop. These low voltages can result in low amplitude signals being output from the VCO. When the VCO output signals fall below a certain level the high speed divider (IC18), stops dividing and therefore it would be impossible to attain VCO lock. To overcome this problem a varicap trigger circuit gives a short duration high pulse to the varicap diodes, thus ensuring that IC18 always functions.

Varicap Trigger Circuit

58 The varicap trigger circuit consists of IC15e, IC15f and associated circuitry. Its purpose is to produce a low pulse on the PC1/PC2 input line to IC19. The pulse has a duration of approximately 150 msecs and will be produced whenever an out of lock indication is present.

59 IC15e and IC15f are connected as an astable multivibrator which functions as follows. The out of lock indication voltage is normally low when loop control is maintained by PC1. Thus D16 is conducting and IC15e pin 1 is pulled low by IC12 pin 4 and R84. IC15e pin 2 is high and D13 is reverse biased. Therefore, the varicap trigger circuit is disabled and has no effect on loop filter operation. The high on IC15e pin 2 is also fed to IC15f pin 3, putting a LOW on IC15f pin 4 output. As C62 has both ends at 0 V there is no charge on it.

60 Once an out of lock voltage is present, D16 is reverse biased and C62 starts to charge via R86. After an interval of less than one time constant of this charging circuit, IC15e changes state and IC15e pin 2 goes low. This forward biases D13 and IC19 pin 2 is pulsed low producing an inverse pulse that is applied to the varicap diodes D6-D9. The low on IC15e pin 2 also causes IC15f to change state, resulting in a high on IC15f pin 4. C62 now discharges via R86. Once the voltage at the junction of C62, R86 and D16 falls below the threshold of IC15e, it changes state again allowing PC2 to try to attain VCO lock. If lock is not achieved, the cycle will repeat.

AUTO-NULL CIRCUIT (Fig 3.4.4)

61 The purpose of the Auto-nulling loop is to adjust the amplitude of the signal fed to the MOD input of IC12. This ensures that any ripple present on the PC1 output voltage due to phase-jitter is nulled across the total Synthesiser output frequency range. To do this the Auto-null circuit generates a variable dc voltage which is fed to the MOD signal generator (IC16) via the Vref input pin.

62 Operation of the circuit is as follows. The IC12/PC1 output voltage is fed to the non-invert pin of B/IC4 via PL3 pin 20. B/IC4 is a variable gain amplifier whose gain is set by switched attenuators.

$$\text{Approximate gain of B/IC4} = \frac{\text{R8 + (R1 to R6)}}{\text{(R1 to R6)}}$$

R1 to R6 are selected by the 10s and 1s of MHz logic code present on IC3 output pins 4, 5, 6, 7, 14 and 13. These logic levels are used as enable high inputs to B/IC2 and B/IC3a. A high on any of the enable inputs to B/IC2, B/IC3a causes +6 V to be switched to the appropriate attenuator resistor. For example, a high on B/IC2 pin 5 (E1) switches +6 V onto the output terminal pin 3 (Z1), thus R3 is selected.

63 The ripple present on the PC1 output, and therefore present at B/IC4 pin 3, is larger in amplitude at low VCO frequencies than at high VCO frequencies. Thus, by switching the gain of B/IC4 over the total range, its output remains relatively constant. The amplified ripple on B/IC4 pin 6 is ac coupled to the unity gain buffer, B/IC5 by C1. C6 and R10 maintain the stability of this buffer stage, which superimposes the amplified ripple voltage on a dc level of +5 VA.

64 The ripple voltage on B/IC5 pin 6 is connected to the Y1 and Y2 inputs of B/IC6. This IC contains two switches; a high on the enable inputs (E1 or E2) established a low impedance path between the input and output terminals (Y1/Y2 and Z1/Z2). A low on any of the enable inputs open circuits the related input and output terminals. The enables for B/IC6 are determined by IC7a, which has its output pins, 0_1 and $\overline{0}_1$ connected to B/IC6 pin 6 (E2) and pin 5 (E1) respectively, via PL3/9 and PL3/7. The outputs of IC7a, and therefore the enable inputs to B/IC6, change at the same rate as the 'carry out' pulse present at IC14 pin 12. Therefore, the polarity, with respect to +5 VA, of the Auto-null voltage fed to IC16, changes at this same rate (see Paras 66 and 67). The outputs of IC7a are determined as shown in Table 3.4.4 which is a truth table for this D type flip-flop.

Table 3.4.4 IC7/2 Truth Table

Inputs				Outputs	
Pin 6	Pin 4	Pin 3	Pin 5	Pin 1	Pin 2
SD1	CD1	CP1	D1	01	01
L	L	∫	L	L	H
L	L	∫	H	H	L

H = +10 V
L = 0 V
∫ = positive going transition.
0_1 and $\overline{0}_1$ outputs after clock.

65 When B/IC6 Z2 output is enabled, B/IC7, having unity gain, inverts the signal present at B/IC5 pin 6. However, when B/IC6 Z1 output is enabled, B/IC7 output is of the same polarity as B/IC5 pin 6. B/IC7 pin 6 is dc coupled to B/IC8 via R14.

66 B/IC8 is an integrating op-amp having a very high dc gain, but is a rejection filter to any ac component. Therefore, its output on pin 6 is a dc voltage that is in proportion to the ripple voltage of PC1. The polarity of this voltage, with respect to +5 VA , is dependent upon the state of the enable inputs to B/IC6.

67 The dc voltage on B/IC8 pin 6 is fed to PL3/18 via R16 and the switched attenuator network of R17 to R22. The values of resistance are selected by the 1s of MHz and 10s of MHz data in the same way as the resistors for B/IC4. Table 3.4.5 shows the frequency code-resistance selection for both resistor attenuation networks. The output voltage on PL3/18 is approximately:

$$\text{B/IC8 pin 6 dc voltage} \times \frac{(\text{R17 to R22})}{\text{R16} + (\text{R17 to R22})}$$

Therefore the dc voltage level at PL3/18 is higher at low VCO frequencies than at high VCO frequencies. This voltage is then fed to the Vref input of IC16 via IC17d and LK4. IC17d is a buffer amp of unity gain.

Table 3.4.5 Code/Resistance Selection

F(MHz)	10s of MHz Code		1s of MHz Code				Resistor/s	Resistor/s
	A	B	D	C	B	A	R1 to R6	R17 to R22
1	0	0	0	0	0	1	R1	R17
2	0	0	0	0	0	0	R2	R18
3	0	0	0	0	1	1	R1,R2	R17,R18
4	0	0	0	1	0	0	R3	R19
5	0	0	0	1	0	1	R1,R3	R17,R18
6	0	0	0	1	1	0	R2,R3	R18,R19
7	0	0	0	1	1	1	R1,R2,R3,R4	R17,R18,R19,
8	0	0	1	0	0	0	R4	R20
9	0	0	1	0	0	1	R1,R4	R17,R20
10	0	1	0	0	0	0	R5	R21
11	0	1	0	0	0	1	R1,R5	R17,R21
12	0	1	0	0	1	0	R2,R5	R18,R21
13	0	1	0	0	1	1	R1,R2,R5	R17,R18,R21
14	0	1	0	1	0	0	R3,R5	R18,R21
15	0	1	0	1	0	1	R1,R3,R5	R17,R18,R21
16	0	1	0	1	1	0	R2,R3,R5	R18,R19,R21
17	0	1	0	1	1	1	R1,R2,R3,R5	R17,R18,R19,R21
18	0	1	1	0	0	0	R4,R5	R10,R21
19	0	1	1	0	0	1	R1,R4,R5	R17,R20,R21
20	1	0	0	0	0	0	R6	R22
21	1	0	0	0	0	1	R1,R6	R17,R22
22	1	0	0	0	1	0	R2,R6	R18,R22
23	1	0	0	0	1	1	R1,R2,R6	R17,R18,R22
24	1	0	0	1	0	0	R3,R6	R19,R22
25	1	0	0	1	0	1	R1,R3,R6	R17,R19,R22
26	1	0	0	1	1	0	R2,R3,R6	R18,R19,R22
27	1	0	0	1	1	1	R1,R2,R3,R6	R17,R18,R19,R22
28	1	0	1	0	0	0	R4,R6	R20,R22
29	1	0	1	0	0	1	R1,R4,R6	R17,R20,R22
30	1	1	0	0	0	0	R5,R6	R21,R22

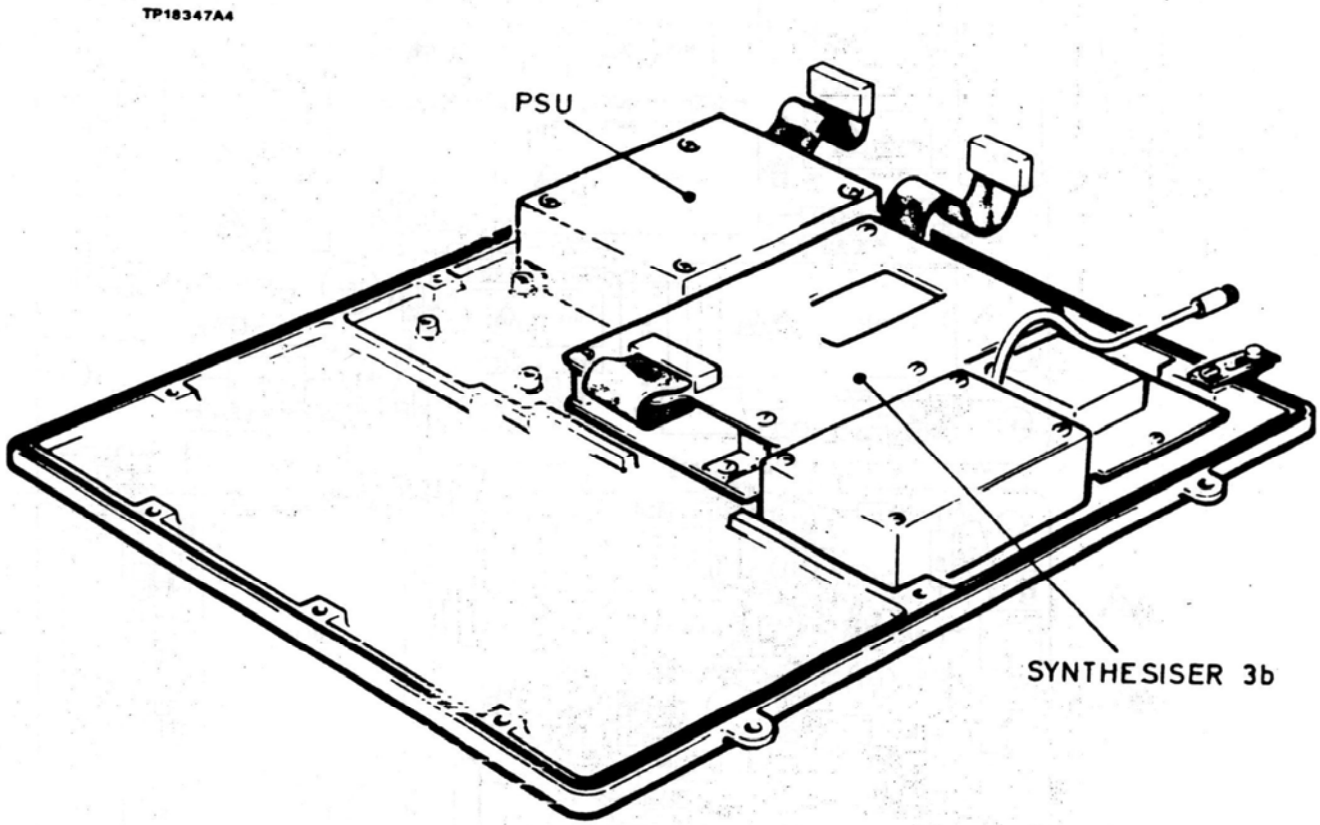


Fig 3.4.1 Synthesiser Lid Assembly

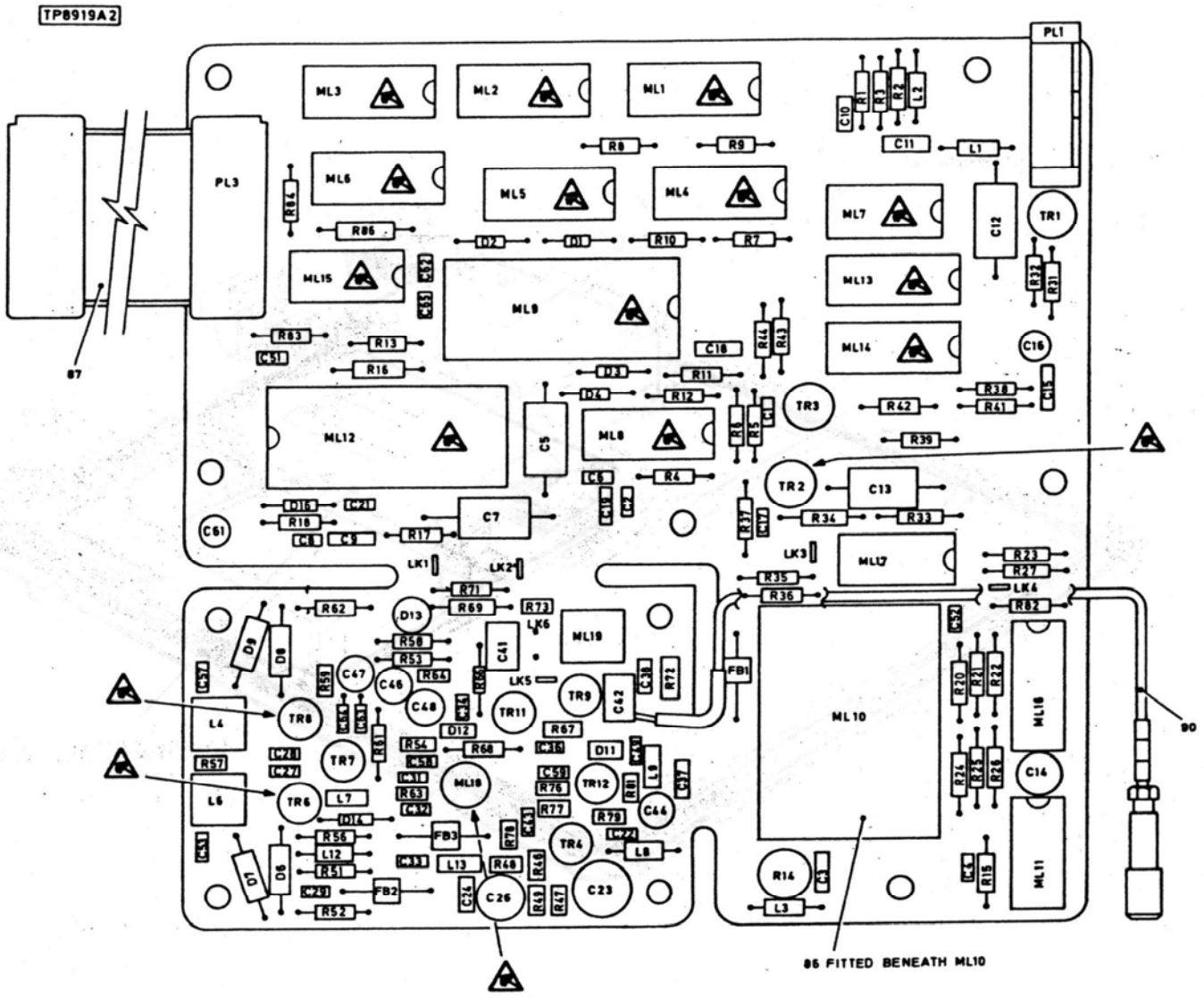


Fig 3.4.2 Synthesiser (VCO) Component Location

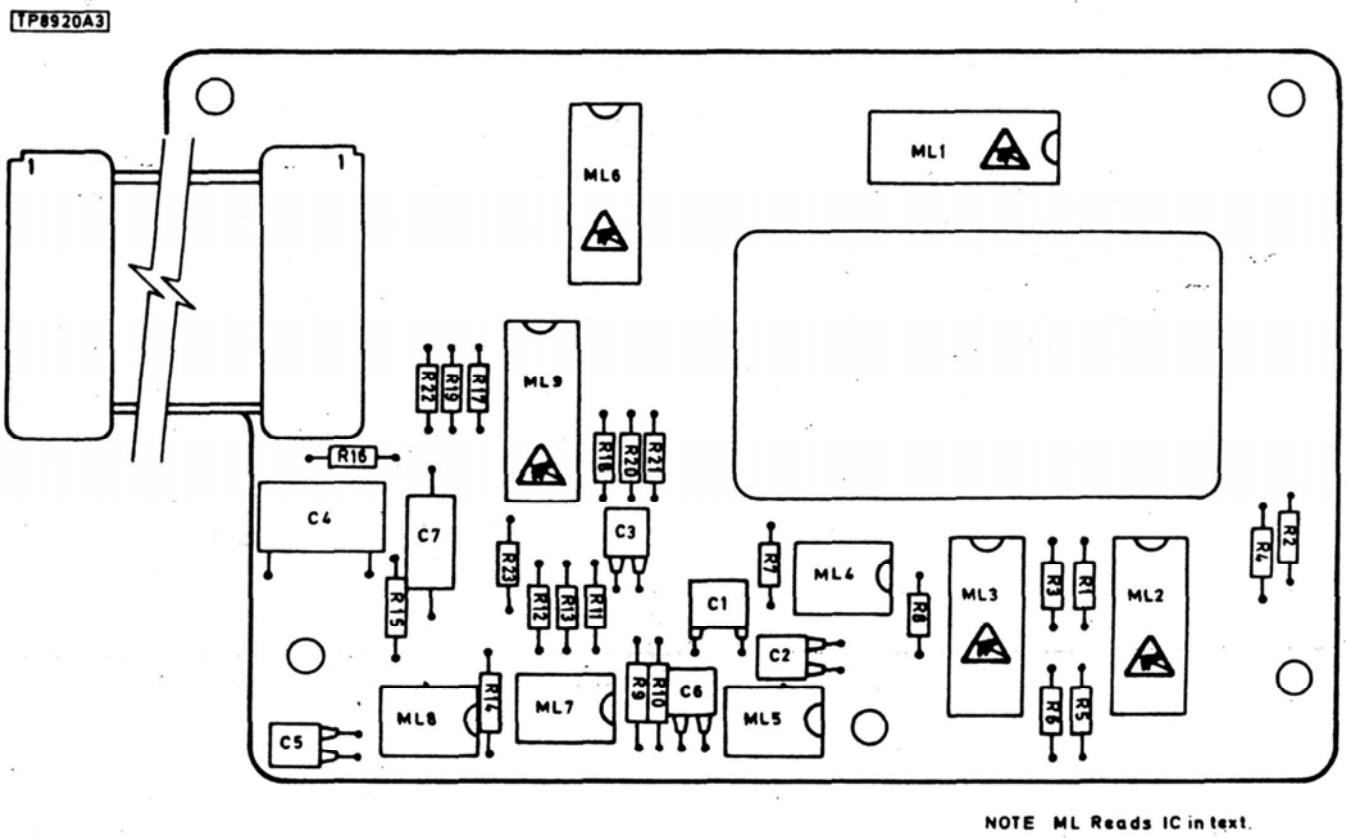
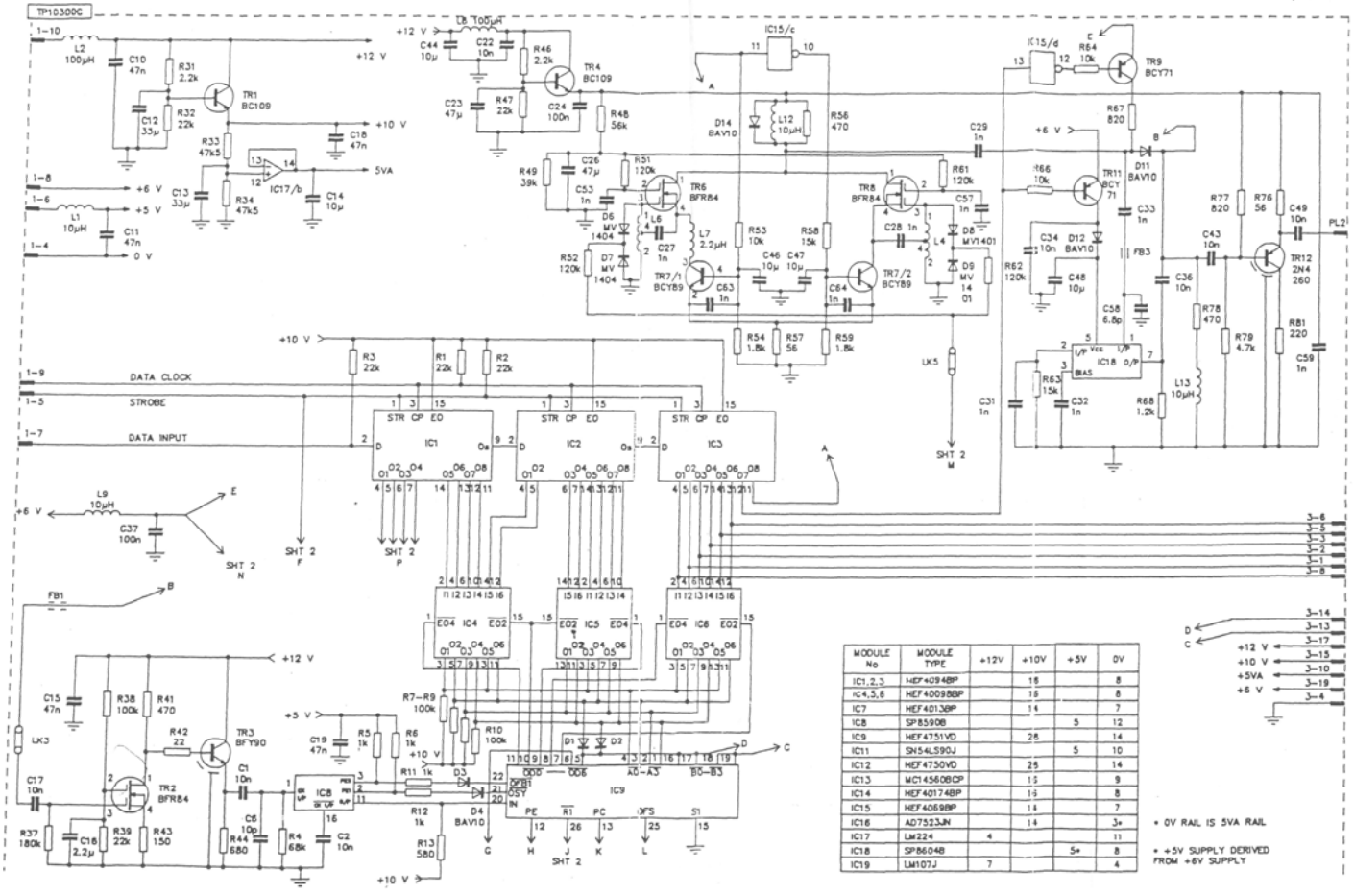


Fig 3.4.3 Synthesiser (Auto-null) Component Location



MODULE No	MODULE TYPE	+12V	+10V	+5V	0V
IC1,2,3	HEF4094BP		16		8
IC4,5,6	HEF4009UBP		16		8
IC7	HEF4013BP		14		7
IC8	SP8590B			5	12
IC9	HEF4751VD		28		14
IC11	SN54LS90J			5	10
IC12	HEF4750VD		28		14
IC13	MC14560BCP		16		9
IC14	HEF40174BP		16		8
IC15	HEF4069BP		14		7
IC16	AD7523JN		14		3*
IC17	LM224	4			11
IC18	SP8604B			5*	8
IC19	LM107J	7			4

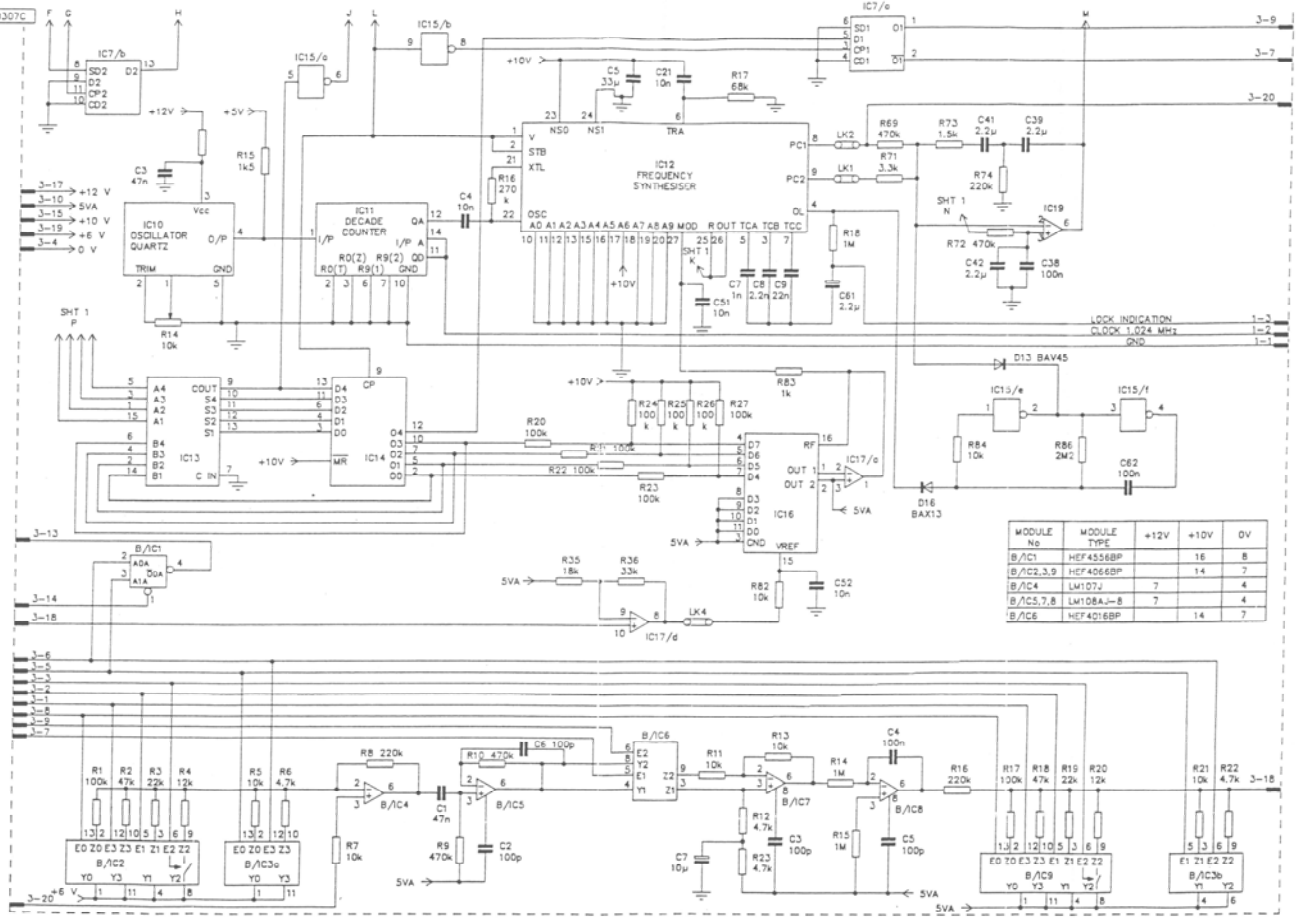
* 0V RAIL IS 5VA RAIL

* +5V SUPPLY DERIVED FROM +6V SUPPLY

3.4.4

Circuit Diagram for Synthesiser 1 (Sheet 1 of 2)

Fig 3.4.4



MODULE No	MODULE TYPE	+12V	+10V	0V
B/IC1	HEF4556BP		16	8
B/IC2,3,9	HEF4066BP		14	7
B/IC4	LM107J	7		4
B/IC5,7,8	LM108AJ—8	7		4
B/IC6	HEF4016BP		14	7

Circuit Diagram for Synthesiser 2 (Sheet 2 of 2)

Fig 3.4.4

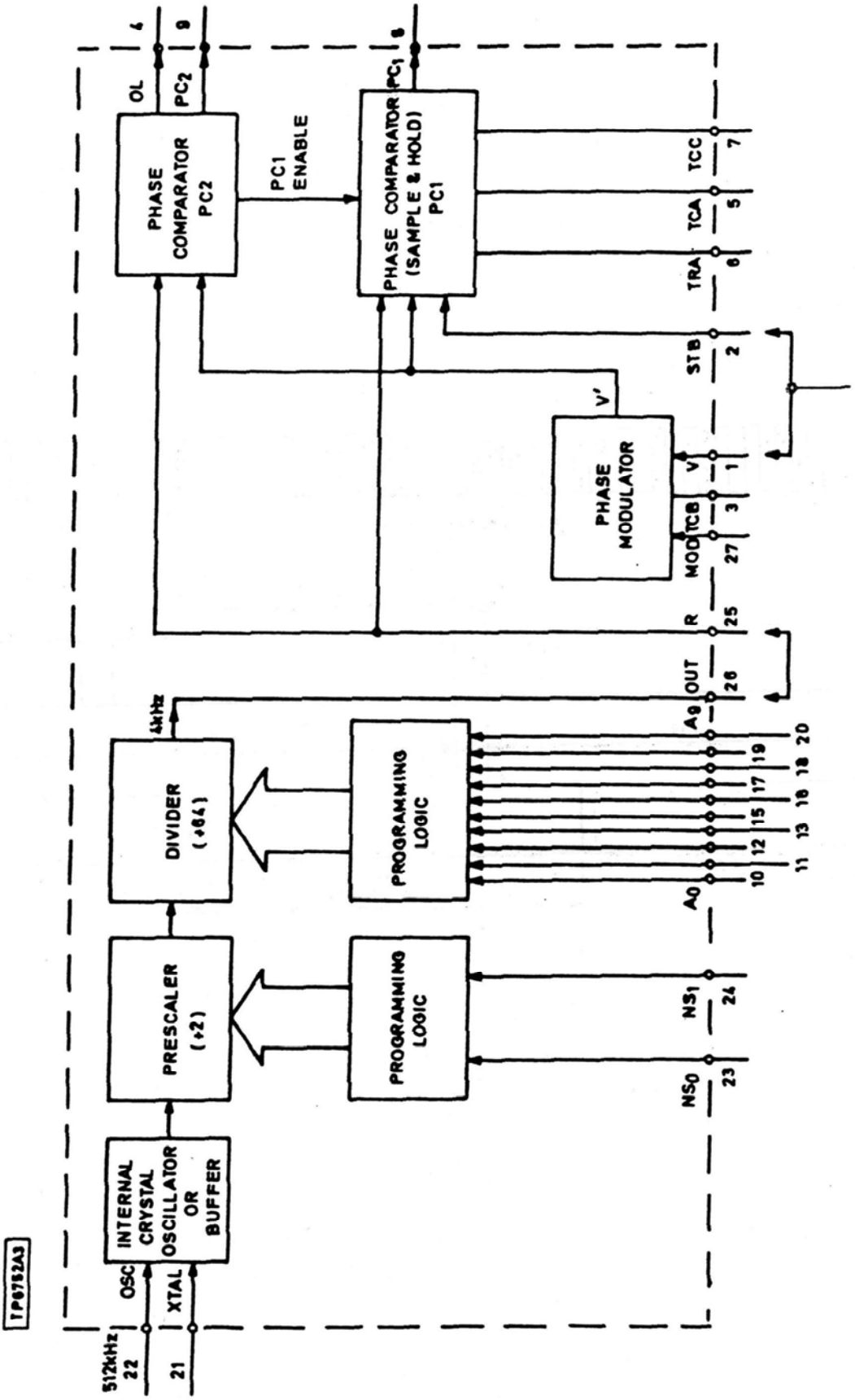


Fig 3.4.5 Block Diagram : Internal Functions of IC12 Frequency Synthesiser

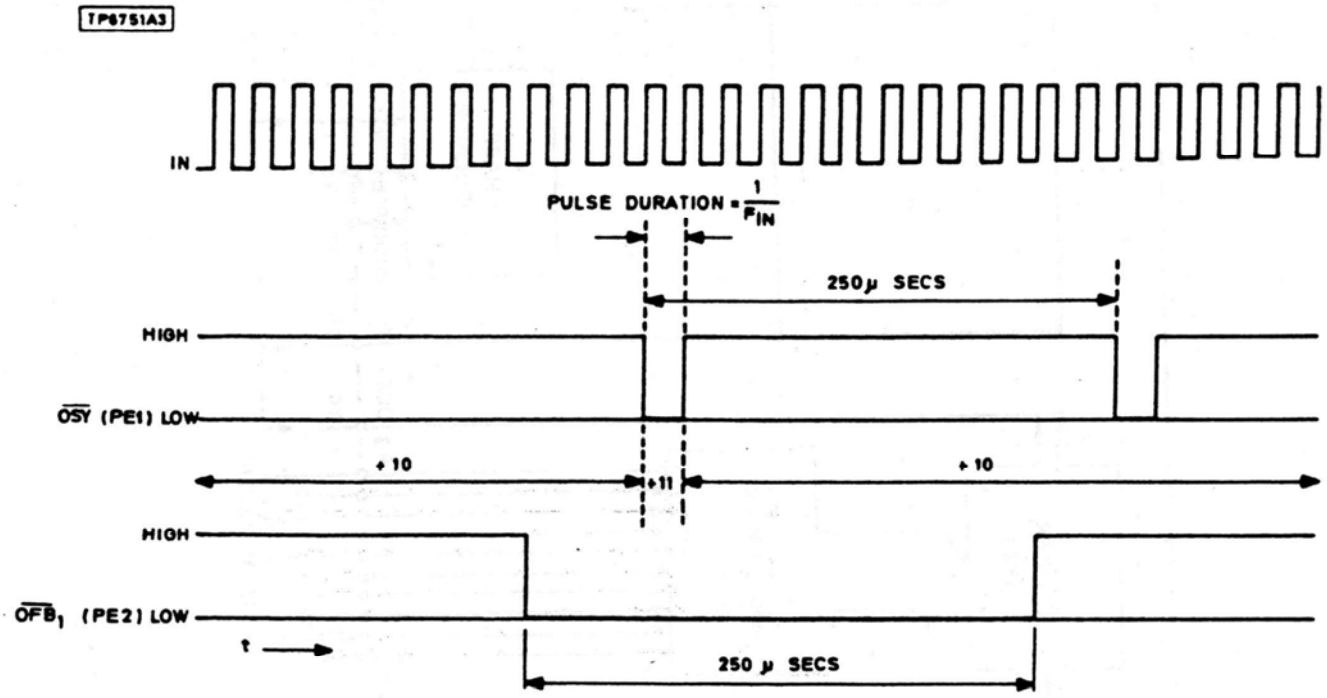


Fig 3.4.6 Timing of IN, $\overline{OSY}$ and $\overline{OFB1}$

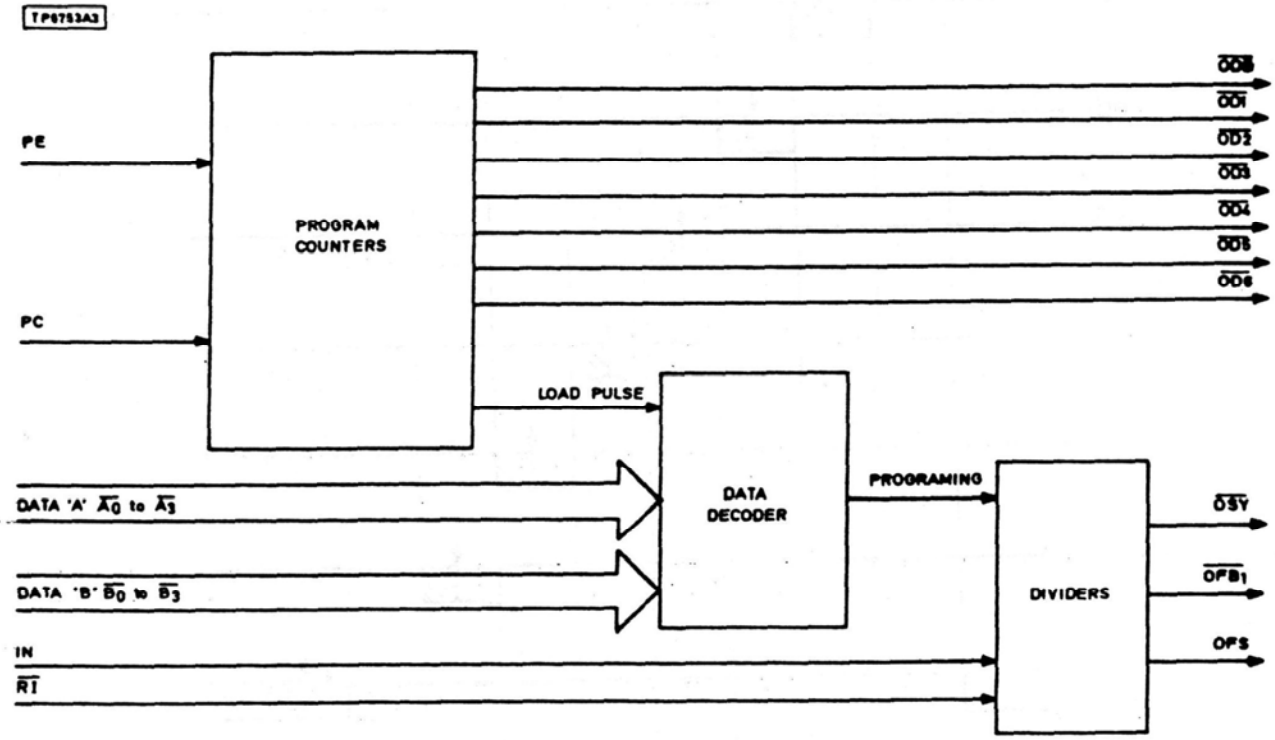
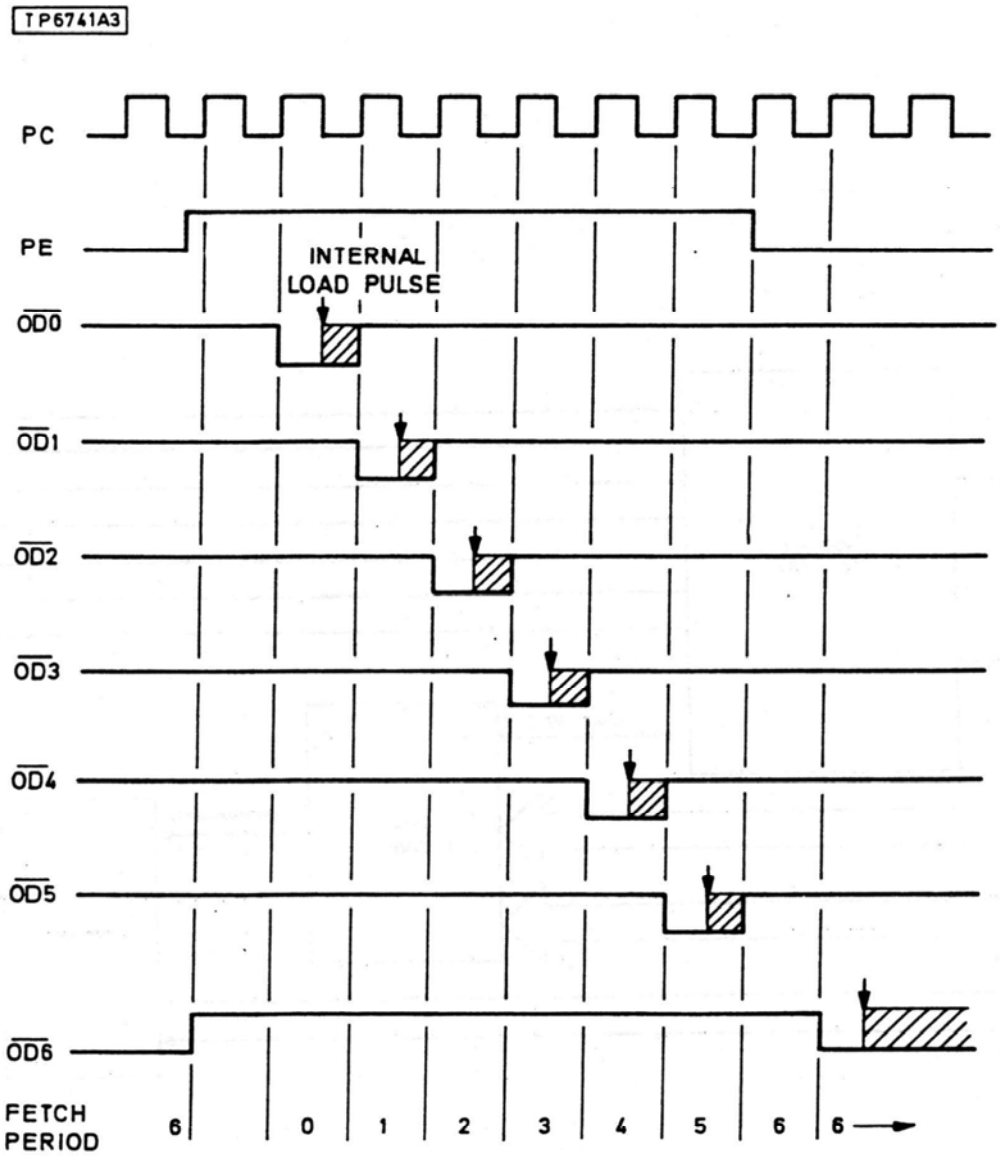
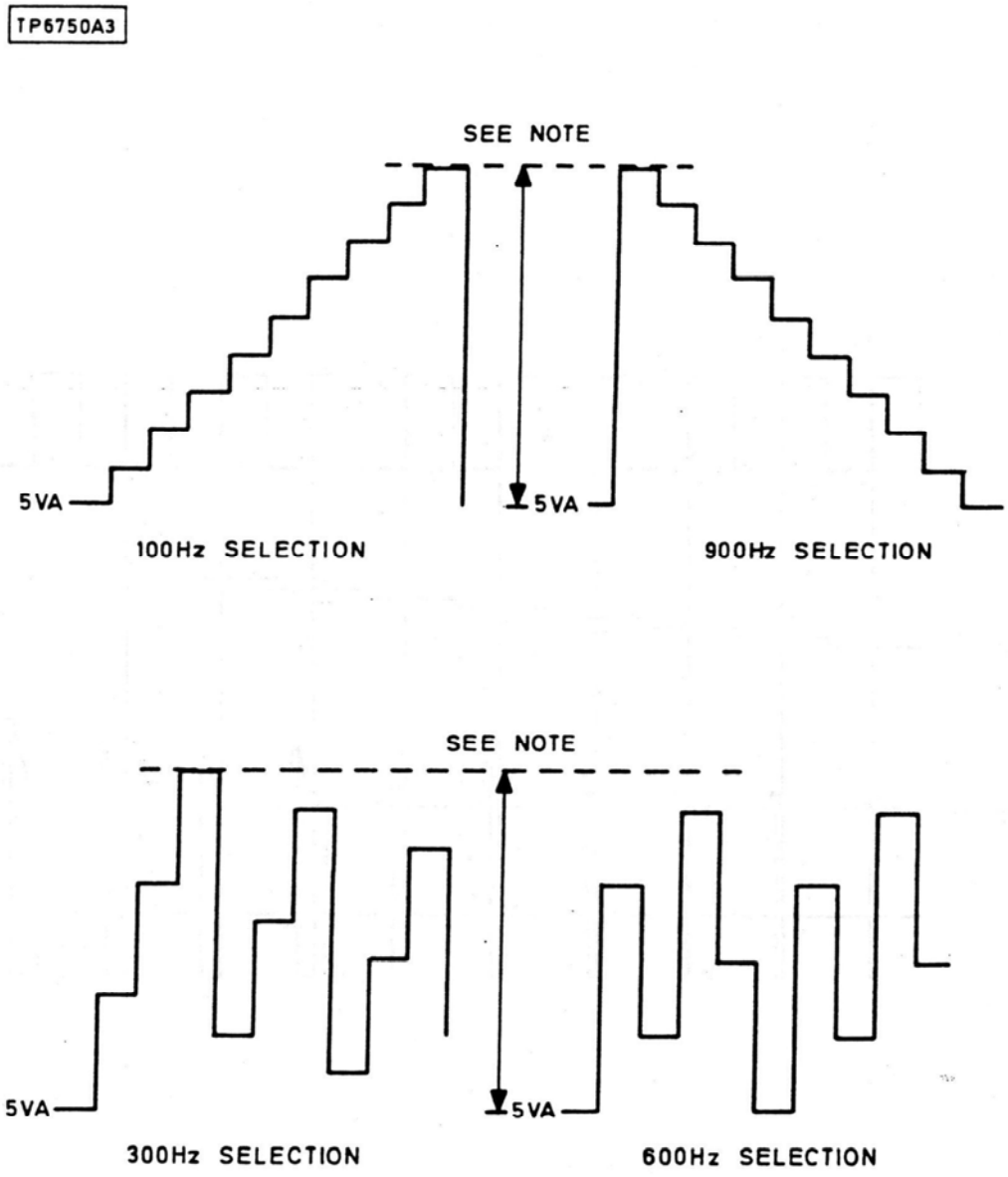


Fig 3.4.7 Internal Configuration of the Universal Divider, IC9



NOTE: DATA IS ENTERED INTERNALLY BY INTERNAL LOAD PULSES DURING SHADED PERIODS.

Fig 3.4.8 Timing Diagram for PC, PE, Load Pulses and Data Address



NOTE.
AMPLITUDE DEPENDANT ON SYNTHESISER OUTPUT FREQUENCY. LOW FREQUENCIES HAVE GREATER AMPLITUDE THAN HIGH FREQUENCIES.

Fig 3.4.9 Idealised MOD Signal Waveforms

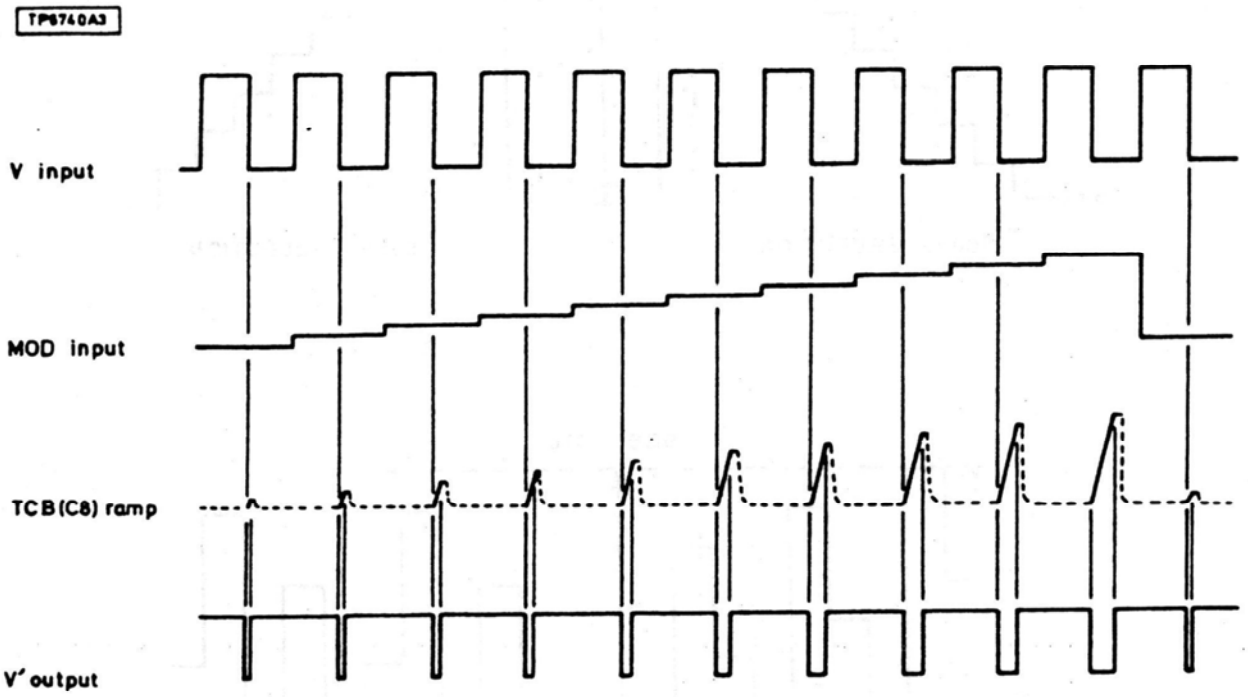


Fig 3.4.10 Example of Signal Relationships of Phase Modulator (100 Hz)

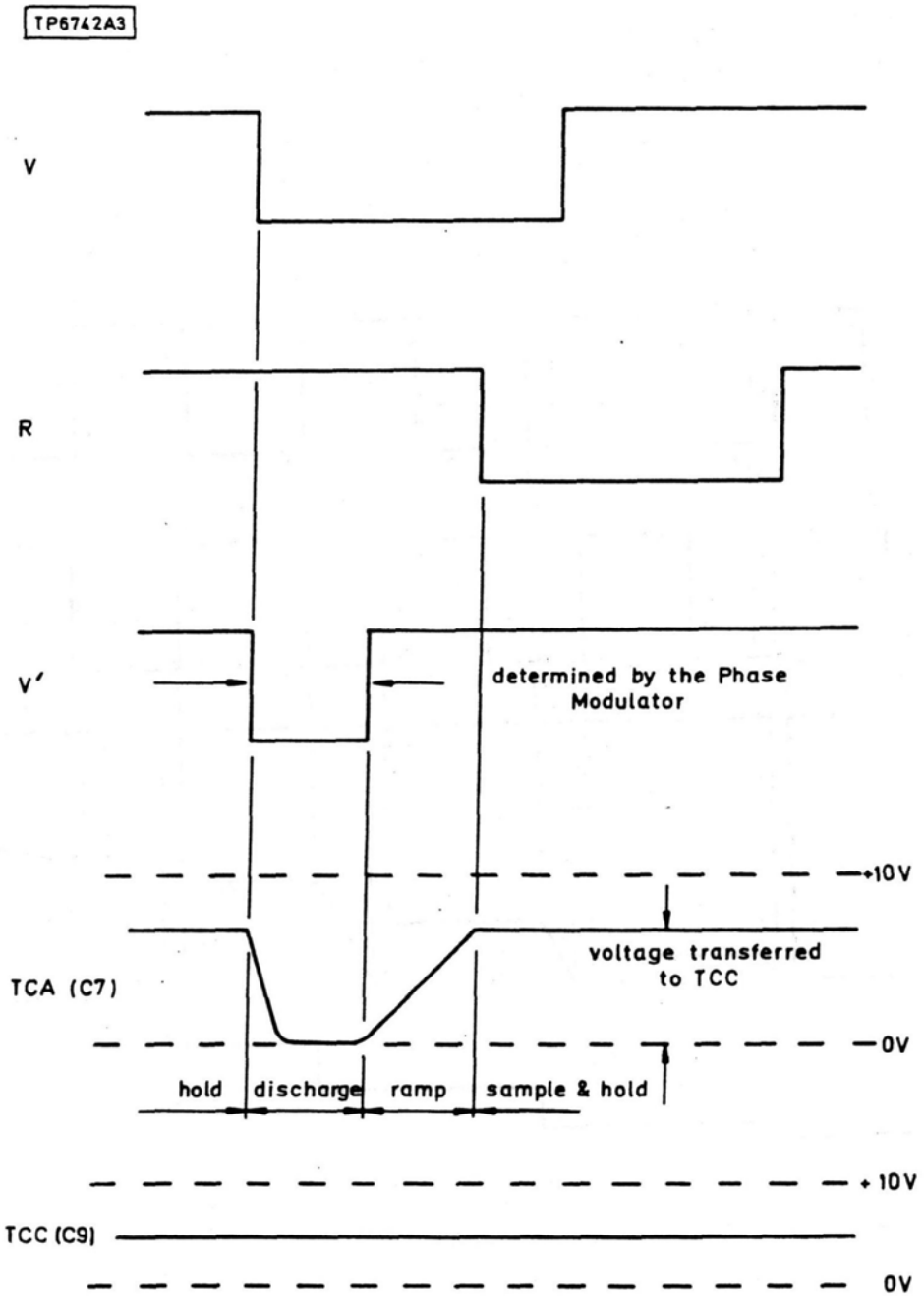


Fig 3.4.11 Waveforms Associated with PC1

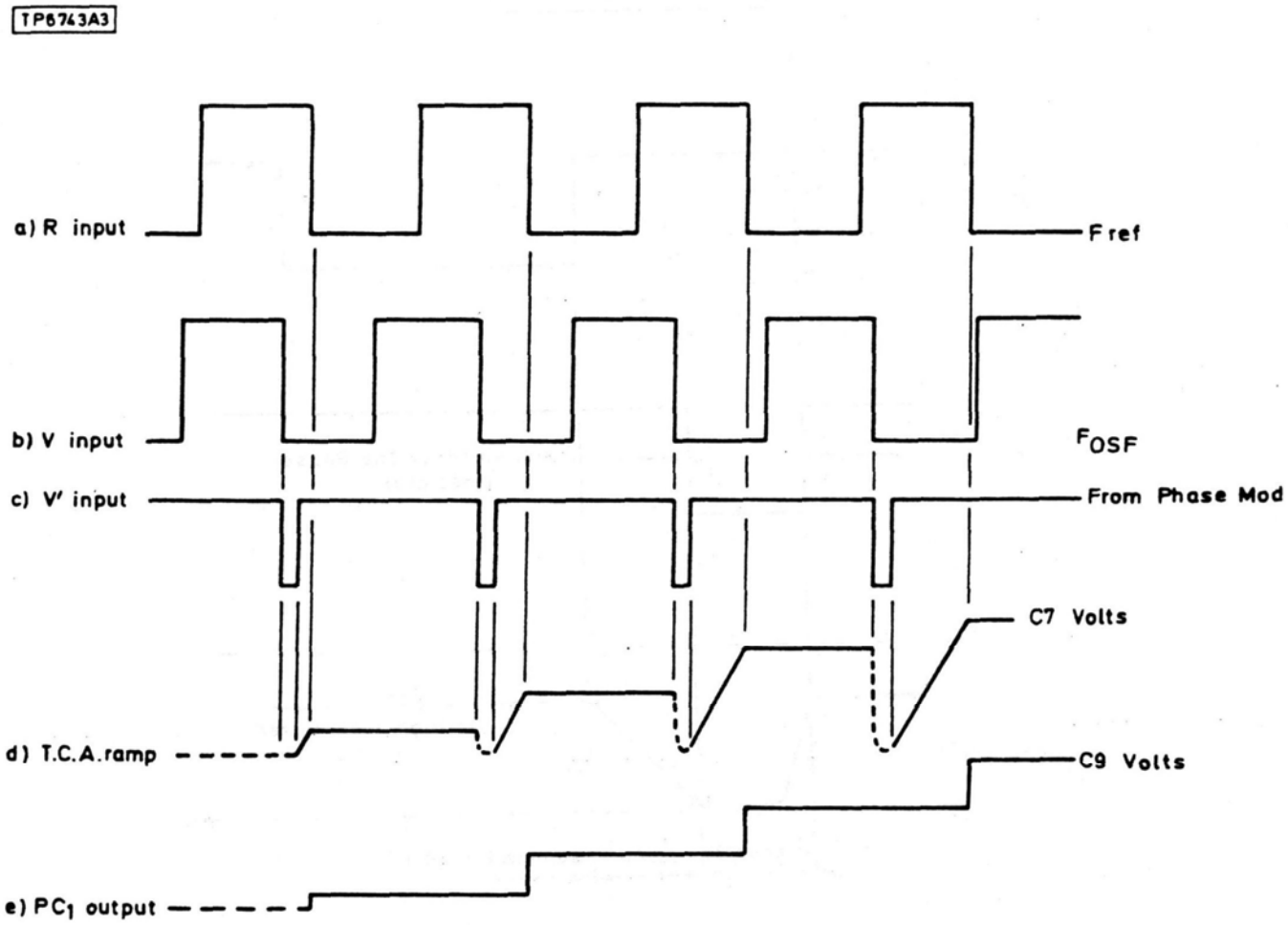


Fig 3.4.12 Theoretical PC1 Waveforms for 100 Hz Selection, No MOD Signal Input

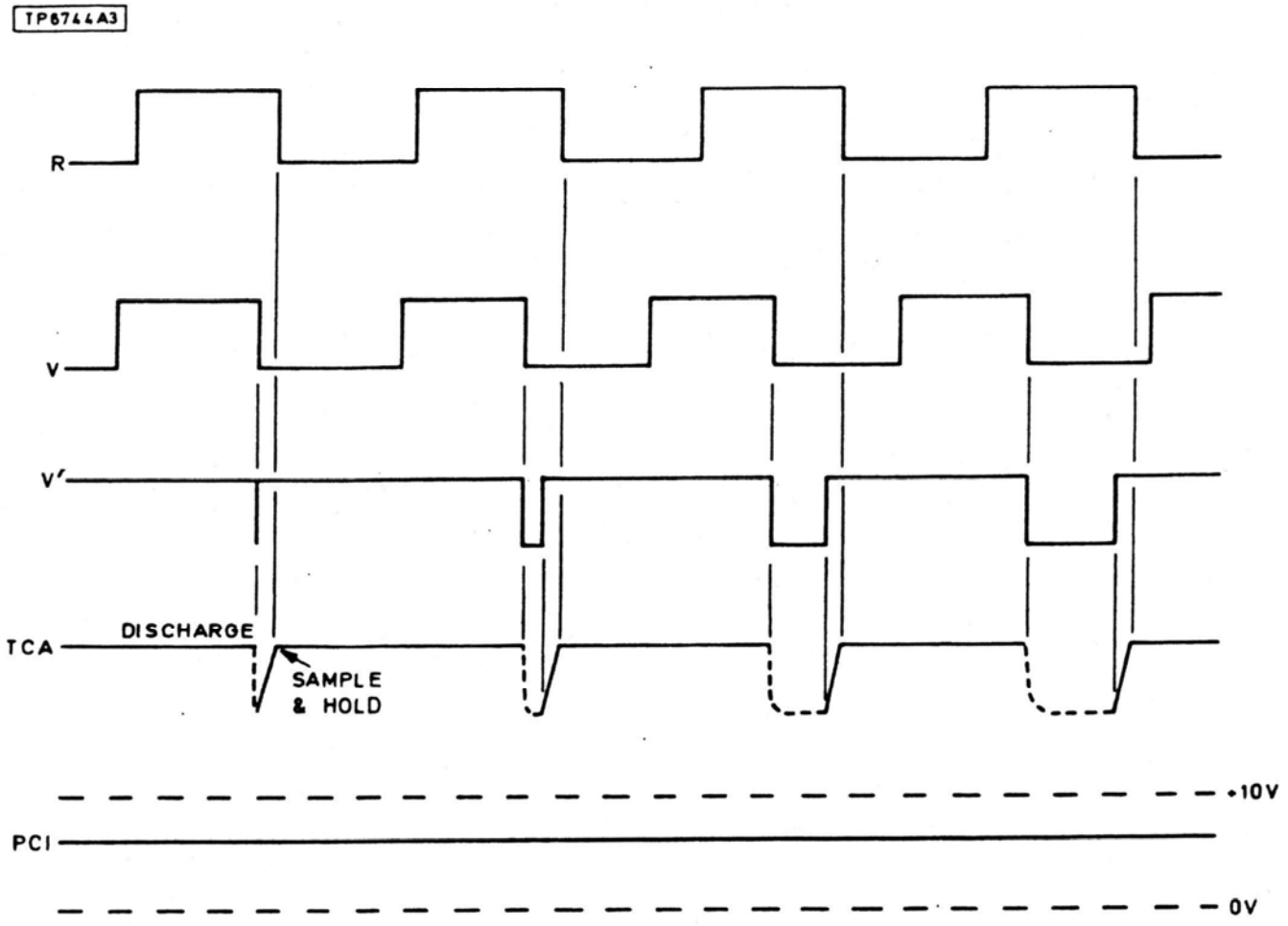


Fig 3.4.13 Theoretical PC1 Waveforms for 100 Hz Selection and MOD Signal Input

CHAPTER 3.5

ANTENNA TUNING UNIT

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CHAPTER 3.5

ANTENNA TUNING UNIT

INTRODUCTION

1 The Antenna Tuning Unit (ATU),(Fig 3.5.1 - Item 2), forms part of the Case Assembly. The unit consists of a Control PEC on which most of the circuitry is located, Filter Assembly, Variable Capacitor Assembly and Coil Assembly (Fig 3.5.2). Chapter 3.0 gives a brief outline of the functional operation of the ATU; this chapter gives a detailed description of the circuit operation.

RF SIGNAL PATH (RECEIVE)

2 The receive signal path is shown in Fig 3.5.4, which shows the points of entry and exit at each sub-assembly within the ATU. What happens to the signal as it passes through each sub-assembly is explained in the following paragraphs.

Coil Assembly (Fig 3.5.6).

3 Switch S2, which is operated by a cam on the motor driver switch S1, connects L2 in series with the antenna on the lowest frequency band. However, L2 has a purpose only in the transmit mode and so may be ignored for the moment. One of the tappings on L1 is selected by S1, which also selects the tapping on T1 appropriate to the selected frequency band. Another section of S1 is the band select switch, which operates to stop the motor when the chosen band is selected; the manner of its operation will be described later. The fine tune variable capacitor is connected across the selected part of L1; the driving of this capacitor is also described later.

Control PEC (Fig 3.5.3 and 3.5.7/8)

4 From the coil, the signal enters the control PEC, passing through isolating capacitors C58/C59, and then out of the control PEC at TB2-2 to the ATU socket. At TB2-2, the signal path is connected to +12 V via the filter network including L4-5-6; C58/C59 isolate the dc from the aerial. Passing through the coaxial link connecting the ATU and RT sockets on the front panel, the signal re-enters the control PEC at PL1/4. The +12 V passes via rf chokes L2 and L7 to PL3, pin 6 and then to Channelisation as amplifier control. The rf signal, now isolated from the dc by C17/C18, passes to the VSWR detector network (explained under 'Transmit' signal path) and the Passive Protection network (D31 to D38, R91 to R96, R22-28-99, C52, C55). A small reverse bias potential applied to the signal diodes in the protection network prevents their conduction under normal reception conditions (otherwise signal quality would be impaired). Any received signal of excessive amplitude overcomes the reverse bias and so the diodes short-circuit such signals. The bias potential is derived from the +15 V Battery Positive Switched supply and fed via R99 to the protection network. A potential of approximately 0.8 V at the cathodes of D34-35-36 is fixed by D37-38 and R22, R28.

5 From the protection network, the rf signal passes via RLB-2 and RLB-1 to SK1, and then to the filter assembly.

Filter Assembly (Fig 3.5.8)

6 This comprises eight separate band-pass LC filters, all of which are tuned during manufacture for optimum response. Inputs and outputs are switched by S1A and S1B, so that the appropriate filter is automatically selected by the coarse tuning system. The coarse tuning drive motor is located in this assembly. From the filter assembly, the received signals pass to the RF Head.

RF SIGNAL PATH (TRANSMIT)

7 In the transmit mode, rf signals follow approximately the same path as that already described, but in the opposite direction. Some differences for the 'transmit' mode are described in their sequence. The transmit path is shown in Fig 3.5.5.

8 From the RF Head the signals pass through the Filter Assembly (para 6) and then to the control PEC via SK1. In the transmit mode, RLA and RLB are energised so contacts RLA-2 and RLB-1 are in the alternative position to that shown in the circuit Fig 3.5.7. The protection network is thus out-of-circuit and the signals from the filter assembly are routed instead to the Power Amplifier via PL3. After amplification, the signals return to the control PEC via PL1 and then through RLA-2 to the VSWR detector. C57 at PL1/3 improves the impedance matching of the input line.

VSWR Detector (Fig 3.5.7)

9 Both the forward and reversed signals present at the junction of C17, C18 and R41 are fed to the centre tap of L3 via the potential divider network R41 and R42. C70 and C71 improve the high frequency performance of this divider. The forward and reverse power dc voltages produced by this VSWR detector circuitry are derived by signal diodes D12 and D39, which rectify the output alternating signals of transformer L3. This transformer is loaded, for effective operation, by R31.

10 The forward power dc voltage produced by the VSWR detectors is fed from the junction of D12 and rf decoupling capacitor C23 to the junction of R38, R6 and R46. R38 and R6 are coupling resistors to the fine tune control circuits contained on the control PEC, they also provide a dc load for D12. R46 is a coupling resistor to PL3-20 from where the forward power voltage is fed to Channelisation.

11 The reverse power dc voltage produced by the VSWR detectors is fed from the junction of D39 and rf decoupling capacitor C24 to the junction of R29, R37 and R1. R29 is the dc load for D39 and R37 is a coupling resistor to the fine tune control circuits. R1 couples the reverse power voltage to Channelisation, via PL3-19.

12 The Tx signal is fed from the VSWR detector circuit to pin 4 on the control PEC via the dc blocking capacitors C17 and C18. Also connected to this point is the Amplifier Control from Channelisation, via PL3-6 and rf chokes L7 and L2. These two signals, are fed out of the ATU to the front panel RT terminal. If the manpack whip antenna is being used the ATU-RT front panel coaxial link feeds these signals back into the control PEC on TB2-1.

13 TB2-2 has +12 V fed onto it via R49, L6, L5 and L4, which is then fed to Channelisation via the Tx signal path and the Amplifier Control. This dc voltage is blocked by C58 and C59, so only the Tx signal is fed to the coil assembly via TB2-1 and 2d PL1.

14 Coupling of the Tx signal to the ATU coils, L1 and L2, is performed by T1. The tapping of T1 and the values of inductance are selected during the coarse tune. The Tx signal is fed to the antenna base on the front panel via S2 and 2d1.

COARSE TUNE

Band Decoder

15 A binary encoded representation of the nine ATU frequency bands is input from Channelisation on lines A0-A3 of the control PEC (see Table 3.5.1). These four input data lines are connected to IC6, a 4-to-16-line decoder, which sets one of the nine output lines low, corresponding to the decoded band. The output lines of IC6 are connected to the terminals of the band code switch, which is located on the drive shaft of the band motor in the coil assembly.

Table 3.5.1 Band Codes

FREQUENCY (MHz)	BAND	PL3 10	PL3 11	PL3 12	PL3 13
		A_0	A_1	A_2	A_3
1.6 - 1.9	1	1	0	0	0
1.9 - 2.8	2	0	1	0	0
2.8 - 4.2	3	1	1	0	0
4.2 - 6.3	4	0	0	1	0
6.3 - 9.4	5	1	0	1	0
9.4 - 14	6	0	1	1	0
14 - 20	7	1	1	1	0
20 - 27	8	0	0	0	1
27 - 30	9	1	0	0	1

Band Code Switch

16 When the tuning system is static the band code switch wiper is at logic 0, but when a change in frequency band is demanded, the switch wiper changes to logic 1 and the switch contact corresponding to the wanted band changes to logic 0. The switch wiper is connected to control PEC pin 6 so, when this is at logic 1, both inputs to AND gate IC11c are at logic 1 so its output is also logic 1.

Note: IC11c pin 8 is only at logic 1 after a delay whose length is determined by R77 and C46, this is to prevent the band motor from turning when the Callpac is switched on.

Band Motor Drive (Fig 3.5.7)

17 The band motor drive circuit comprises TR9, TR11, TR12 and their associated components. TR9 is normally off and so TR11 is also off. When the output from IC11c goes high, this is inverted by IC1e so switching TR9 on. Base current is then available for TR11 so

it too is switched on and the band motor circuit is completed. TR12 is concerned with motor braking as described in para 19.

Band Motor

18 Motor M1 (located on the Filter Assembly) drives the following components.

(a) Bandpass Filter Switches, S1A and S1B, on the Filter Assembly,

(b) ATU Coils, L1 and L2
(c) ATU Matching Transformer, T1
(d) Series Inductor Select Switch, S2,
(e) Band Code Switch, S1.

) All on the Coil Assembly

One of the contacts of S1 (determined by the band decoder) is at logic 0. When the motor has driven S1 to this position, the logic 0 is conveyed via 2a-6 to the control PEC pin 6 and IC11c, which is thus disabled. TR9 is then turned off and the motor stops.

Motor Braking

19 To prevent overshoot of the coarse tune point, regenerative braking of the motor is applied. When the band motor is running, TR11 is on so D16 is conducting, which ensures that TR12 is biased off. When the band motor drive current is switched off, by TR9 base going high, D16 stops conducting and TR12, being no longer biased off, is switched on by the back emf of the motor. With TR12 on, the stored energy from the motor windings is rapidly dissipated through R57, (the collector load of TR12) so motor braking is very efficient. The function of D17 is to protect the current supply transistor TR11 and the braking transistor TR12 against excess reverse voltages due to sparking at the motor brushes.

Bandpass Filter Switches (Fig 3.5.8)

20 The bandpass filter switches S1A and S1B, mounted on the filter assembly, are rotated by the drive shaft of M1 to select one of the eight bandpass filters on the two PECs in the filter assembly. Bands 1 to 4 filters are on PEC 2ba and bands 5 to 8 filters are on PEC 2bb.

ATU Coil Assembly (Fig 3.5.6)

21 The coils, switches and transformer contained in the coil assembly are all driven during coarse tune by the band motor. L1 is fixed and the motor drive shaft and has 4 sets of switches attached to the ends of the coil, so that as the switch shaft rotate the contacts are open-circuit or short-circuit for switched inductance selection in nine frequency bands. L1 (pin 2 to 3) is in circuit only on the lowest frequency band; it is a series loading coil to limit the peak voltage across the variable tuning capacitor located in the Variable Capacitor Assembly. L1 is bypassed for the other eight bands to avoid loss of efficiency through parasitic stray capacitance and is switched by S4. Switches S4 and S3 rotate to short-circuit the coils not-in-use for each of the nine bands (see Table 3.5.2). The coil assembly also includes T1, which is switched in three bands by S2 to match the required 50 ohms impedance at all frequencies. Operation of the band code switch S1 has been explained in para 16. (See also Table 3.5.1).

FINE TUNE (Fig 3.5.7 and 3.5.9)

22 Most of the fine tune circuitry is contained on the control PEC, only the variable tuning capacitor, LED transistor combinations and capacitor motor being on the variable capacitor assembly (Fig 3.5.9). To help the understanding of the logic switching, the pertinent logic states existing prior to a fine tune sequence are given. These logic states are true both for switch-on of the Callpac and when the Callpac is already in operation.

23 Both halves of the automatic fine tune latch (IC7a and b), are reset and the $\overline{Q}$ and Q outputs are at logic 1 and 0 respectively. IC7a and b is reset either during the last fine tune or when the Callpac was switched on. The reset action that occurs during fine tune is explained later in the text, but when the radio is first switched on +5 V is fed to IC7a and IC7b reset inputs via C48, R44, C27 and C25. The logic 1 present on IC7b, $\overline{Q}$ is connected to the triple-input NAND gate IC14a, whose other two inputs are also at logic 1. These two inputs are the manual reverse and manual forward lines (PL3-2 and PL3-7), which are always at logic 1 unless a manual fine tune sequence is in operation. With all of its inputs at logic 1, IC14a output is low and so the output of IC14b is high. The high output from IC14b causes a brief high at IC12a (pin 2) the purpose of which is concerned with capacitor motor braking and is explained later (para 44); the logic level at IC12a pin 2, quickly returns to 0. Since the other input to IC12a is low (being the inverted output from IC14b), its output is low. This is connected to D25 (one half of the diode OR input to IC11a) and as D27 also has a logic 0 on it, the output of IC11a is low. This is applied to the base of switching transistor TR13, whose function is to switch in the dc supply for the Motor Drive circuits (IC13, TR18, TR17, TR23 etc) and to energise the LED/photo transistor pairs. In the condition being considered, TR13 is switched off and the capacitor motor cannot run.

Reverse to Endstop

24 To start the automatic fine tune sequence either the pressel on the handset is keyed or the CALL button is depressed. This operator action results in a brief negative-going pulse at the retune input, PL3/1. This causes a logic 1 to set IC7a, one half of the automatic fine tune latch, and to set the motor direction latch (IC4b). The resulting high from the Q output of IC7a is used to set IC7b.

25 The logic 0 from IC7b ($\overline{Q}$) produces a 1 at the output of IC14a, which is connected to the diode OR input of the AND gate (IC11a). As IC11a pin 1 is already at a 1 the output changes to a logic 1, which turns TR13 on. The collector of TR13 is connected to TB4-3, which in turn is connected to TB4-4, via two LEDs mounted on the variable capacitor assembly (Fig 3.5.9). TB4-4 is connected to the base of TR14, via R82, when TR13 is switched on, it switches TR14 on, thus providing a dc supply for the capacitor motor drive circuits (IC13, TR17, TR18, TR22, TR23 etc). When TR14 is switched on, its base current also energises the series LED in the base circuits of TR1 and TR2 on the variable capacitor assembly turning them on. Once these are switched on, the Reverse Stop and Forward Stop inputs of the control PEC (TB3-3 and TB3-4) go low.

26 The reverse stop input is connected to NAND gate IC8a, producing a logic 1 at its output. This is connected to one input of the dual-input NAND gate of IC9d, whose other input is also at logic 1, so its output is 0. This results in the logic 1 already present on the RF CW Demand line being maintained, ensuring that there is no rf generated during the reverse to endstop sequence.

Table 3.5.2 ATU Band Switching of L1 Coil Assembly

FREQUENCY MHz	ATU BAND	L1 2-3	L1 5-6	L1 6-7	L1 7-8	L1 8-9	L1 9-10	L1 10-11	L1 11-12	L1 12-13
1.6 to 1.9	1	IN CCT	IN CCT	IN CCT	IN CCT	IN CCT	IN CCT	IN CCT	IN CCT	IN CCT
1.9 to 2.8	2	S/C S4	IN CCT	IN CCT	IN CCT	IN CCT	IN CCT	IN CCT	IN CCT	IN CCT
2.8.to 4.2	3	S/C S4	S/C S3F	IN CCT	IN CCT	IN CCT	IN CCT	IN CCT	IN CCT	IN CCT
4.2 to 6.3	4	S/C S4	S/C S3F	S/C S3F	IN CCT	IN CCT	IN CCT	IN CCT	IN CCT	IN CCT
6.3 to 9.4	5	S/C S4	S/C S3F	S/C S3F	S/C S3F	IN CCT	IN CCT	IN CCT	IN CCT	IN CCT
9.4 to 14	6	S/C S4	S/C S3F	S/C S3F	S/C S3F	S/C S3B	IN CCT	IN CCT	IN CCT	IN CCT
14 to 20	7	S/C S4	S/C S3F	S/C S3F	S/C S3F	S/C S3B	S/C S3B	IN CCT	IN CCT	IN CCT
20 to 27	8	S/C S4	S/C S3F	S/C S3F	S/C S3F	S/C S3B	S/C S3B	S/C S3B	IN CCT	IN CCT
27 to 30	9	S/C S4	S/C S3F	S/C S3F	S/C S3F	S/C S3B	S/C S3B	S/C S3B	S/C S3B	IN CCT

27 All of the inputs to IC14b are at logic 1, therefore its output is low and pins 2, 6 and 8 of IC12 remain low. The other inputs of IC12 are logic 1 on pins 5 and 1 and a logic 0 on pin 9. Therefore, the outputs from IC12 are as follows: IC12b is high; IC12a is high and IC12c is low. The outputs from IC12a and b are connected to the NAND gate IC3a, whose output is therefore low. The outputs from IC12a and c are connected to the NAND gate IC9b, whose output is therefore high. The output states of IC3a and IC9b determine the direction of the motor drive current and are connected to the capacitor motor drive circuit.

28 This circuit consists of an astable multivibrator (TR16, TR22 and associated circuitry), two comparator op-amps (IC13) and two pairs of complementary driving transistors (TR17/TR21 and TR18/TR19). The astable multivibrator governs the speed of the capacitor motor by switching TR23. When the astable multivibrator is turned off, by either D22 or D21 conducting, then TR23 is always on and the capacitor motor runs fast. In reverse to endstop sequence D22 is conducting because of the logic 0 present at its cathode, produced by IC11b.

29 With the conditions as stated in para 27, the output of comparator IC13b is high, whilst the output of comparator IC13a is low. These two comparator outputs are connected to the bases of the motor drive transistors and with the outputs as described TR18/TR19 are on, and TR21/TR7 are off. So a drive current is supplied to the capacitor motor (M1 on the Variable Capacitor Assembly) via TR18, TB4-2 M1, back into the control PEC on TB4-1 and then to TR23, via TR19. With the current flowing in this direction the variable tuning capacitor is driven in reverse until the cam mounted on the motor drive shaft interrupts the energising beam of the reverse stop LED. Once this beam is interrupted, TR1 (on the Variable Capacitor Assembly) is switched off and the reverse stop input to the control PEC goes to a logic 1.

30 The logic 1 on the reverse stop input line changes the output of IC8a from 1 to 0. This puts a low on one of the inputs to the motor enable gate (IC14b), which then results in a low output from IC12a and high outputs from IC3a and IC9b. As both of these outputs are at the

same logic level both halves of IC13 have the same output voltages, which switches the motor drive transistors off. This removes the motor drive current, stopping the variable tuning capacitor at the reverse endstop. Note that TR13 is still switched on by the logic 1 at IC11a derived from the logic 1 output from IC14a.

Generation of Low Power CW Tx Signal

31 The logic 0 output from IC8a (due to the 1 on the reverse stop input) is also fed to IC9d and IC14c. IC9d outputs a logic 1 and, since the other inputs to IC14c are also at logic 1, its output is low. This is fed out of the ATU on the RF CW Demand line (PL3-6) to Channelisation, which processes this information and puts the Callpac into the Low Power CW Transmit mode.

Note: Both halves of IC7 and the motor direction latch (IC4) remain set, even though the retune pulse has now been removed and the retune input has reverted to a logic '1'.

32 When Tx mode is required Channelisation puts the $\overline{\text{Tx}}$/Rx select input to the control PEC (PL3-9) low. This is inverted by IC1b putting a logic 1 onto one input of AND gate IC11d. The other input to this gate is also at a logic 1, therefore its output is high and TR8 is switched on. This energises RLA and RLB, which puts them into the Tx position. The protection latch (IC4a), is reset by the logic 1 present on the $\overline{\text{Tx}}$/Rx select line before the relays take up the Tx mode.

Fast Forward Traverse

33 The Low Power CW Transmit signal is fed through the ATU (as described in paras 7 to 14) and passes through the VSWR detector circuits (control PEC), which produce forward and reverse power dc voltages. The forward power dc voltage is fed via R6 to the base of TR1, turning it on. After approximately a 1.5 second delay, due to the discharge circuit of C4 and R3, IC1a outputs to a logic 1. The delay is incorporated to allow the rf signal to stabilise.

34 The logic 1 from IC1a resets IC7a (part of the automatic fine tune latch) and its $\overline{\text{Q}}$ output, now high, is inverted by IC9a (whose other input is high). Another inversion by IC8c resets the motor direction latch (IC4b). The logic 0 on IC4b pin 13 produces a 1 at IC8a pin 3 so, with all of the inputs to the motor enable gate (IC14b) high, the output of this gate goes low. Therefore, the inputs to the triple OR gate IC12 are logic 0 on pins 2, 5 and 8 and logic 1 on pins 1 and 9. Thus IC3a output is high and IC9b output is low. The logic states of IC3a and IC9b are now opposite to their states when reverse travel was required.

35 The logic 0 from IC9b is fed to the inverting input of comparator (IC13a), so its output goes high. With the low already output from IC13b, the capacitor motor drive current now flows via TR17 and TR21, thus the variable tuning capacitor is driven in the forward direction. The capacitor motor runs at the fast speed because the astable multivibrator is turned off by the logic 0 at IC11b, which provides a conducting path for D22. The low output from IC11b results from the inversion (by IC1c) of the logic 1 output from the threshold detector (IC2a) when the tuning rf signal is first generated (paras 36 to 38 give further details).

Slow Forward Traverse and Tune Point Detection

36 At the start of a fine tuning sequence there is bound to be some mismatch of the Antenna, so forward and reverse power levels will be detected by the VSWR circuits. As the

tuning point is approached, reverse power voltage falls and forward power voltage increases. These two voltages are fed to the differential input of IC2d, which provides an output relative to the ratio of forward power and reverse power Pf/Pr, and is at a maximum when the Antenna is correctly matched and tuned.

37 The forward power and reverse power dc voltages derived by the VSWR detectors drive current through a pair of matched diodes, TR3, via R37, R38 and R39. As the voltage drop across a diode has a logarithmic relationship to the current through it, the inputs to IC2d are: at pin 12 : log Pf and at pin 13 : log Pr. Therefore its output is log Pf - log Pr which is the ratio of forward power to reverse power. This output is largely independent of changes in common power input levels, but is affected considerably by changes in the relative levels of the inputs. This means that IC2d output is low at the start of a tuning sequence but increases as the matching is improved.

38 IC2d output is connected directly to IC2a inverting input, which is used as a threshold detector to select fast or slow capacitor motor speed. When the ratio Pf/Pr increases, IC2d output goes high and once this voltage is above the threshold set by R30, IC2a output changes state; ie goes low, which in turn biases D22 off, via IC1c and IC11b. Thus the astable multivibrator runs and the 'on' time of TR23 is halved thereby reducing the rate of drive current through the motor, which then runs at the slow speed.

39 The output from the differential amplifier (IC2d), is also fed to the tune-point detection network of IC2b and IC2c and associated components. IC2b is a voltage-follower that together with D2 on the output acts as a peak detector. As the tune point is approached the voltage on the non-inverting input of IC2b increases and, because of the voltage-follower action, IC2b output also increases. This forward biases D2, charging C11 and C12, which store the peak value of the forward-to-reverse power ratio. This stored peak value is connected to pin 9 of IC2c via R17, whose other input, pin 10, is the instantaneous value of the forward-to-reverse power ratio.

40 IC2c compares the varying instantaneous value of the forward-to-reverse power ratio with the stored peak value. Just after the tune point, ie as the instantaneous value on pin 10 falls below the stored peak value on pin 9, the output from IC2c goes low. This low resets one half of the automatic fine tune latch (IC7b), via IC9c and R68. The logic 0 on the Q output is fed to IC9a and IC14c, so both outputs go high, thus removing the low on the RF CW Demand line and the reset logic for the motor direction latch (IC4b).

41 The logic 1 from IC7b $\overline{Q}$ changes the logic state from IC14a from high to low. This puts a low onto one of the inputs of the motor enable (IC14b) so its output changes to a 1. This is inverted by IC1d putting a 0 onto IC12a so, as the other input to this EXCLUSIVE-OR is also at 0, IC12a output goes low. This is fed via D25 to IC11a, whose output goes low, so turning TR13 off. This removes the dc supply from the motor drive circuits and the capacitor motor stops.

Forward to Endstop

42 If the tune-point is not found the capacitor motor continues to run until the cam mounted on the motor drive shaft interrupts the energising beam of the LED-to-base connection of TR2 on the variable capacitor assembly. When this beam is interrupted, a forward stop signal is produced on TB3-4 of the control PEC, which puts the output of IC8b to low. This removes the enable input to IC14b whose output changes to a 1. This is inverted by IC1d which changes

IC12a output to a 0, and so IC9b and IC3a outputs go high. Resulting in the outputs from both the comparators IC13a and IC13b being the same and the motor drive current is removed.

43 **Motor Braking.** To prevent overshoot of the fine tune point, braking is applied to the capacitor motor. This is done by a very short reversal of motor drive current, the duration of which is enough to stop the motor without allowing it to run in the opposite direction.

44 Whenever IC14b output changes from low to high, the logic 1 appears briefly at IC12 input pins 2, 6 and 8. C36 charges via D18 and R71 and after approximately 100 msecs the logic 1 on IC12a, b and c reverts to 0. D19 and R69 ensure that the potential on the negative plate of C36 does not go below 0 V. For example consider the case when the output from IC14 changes from low to high at the tune-point.

45 The logic 1 from IC14 is connected to IC12, and via C36 and D18, therefore IC12b output goes high, IC12c output goes low, and IC12a output remains high. Thus the outputs from IC3a and IC9b change momentarily to high and low respectively, which are the conditions for reverse drive. When C36 is fully charged, IC12a, IC12b and IC12c revert to their normal states (para 41)

46 **Switch-on Delay.** To prevent the capacitor motor from moving at initial switch-on of the Callpac, IC11a is connected to the +5 V rail via the delay circuit R77 and C46. This ensures that IC11a cannot change its output state for approximately 1.5 seconds, hence inhibiting TR13 and TR14 from being switched on.

Operation Under Manual Control

47 The Antenna can be fine-tuned manually without generating a Tx signal and this is done via the manual forward and manual reverse inputs to the control PEC on PL3-7 and PL3-2, supplied by Channelisation. The manual forward line is connected to the reset input of the motor direction latch (IC4b) via IC8c and R107, whilst the manual reverse line is connected to the set input of IC4b via IC8d. Also the manual forward and manual reverse lines are connected to IC14a so if either of the manual control inputs goes low (as a result of the command generated by Channelisation), IC14a output goes high thus enabling the capacitor motor drive current via logic gates IC14, IC11 etc.

48 The motor direction latch is either set or reset depending upon which manual control line is at logic 0, so the capacitor motor runs in either the reverse or forward direction. Under manual tune, the slow speed is always selected for the capacitor motor because D21 and D22 remain reverse-biased therefore the multivibrator will be running. The capacitor motor continues to move forward or in reverse as long as one of the manual command inputs is at logic 0, but stops if none of these inputs is selected because IC14a does not output a logic 1 unless one of its inputs is at logic 0.

Rx PROTECTION

49 When the Callpac is in Rx mode, the $\overline{\text{Tx}}$/Rx select input (PL3/9) is high. This is inverted by IC1a so the output of IC11d is low and TR8 is therefore off, leaving the relays RLA and RLB in the Rx condition. The high on the $\overline{\text{Tx}}$/Rx line is fed to IC2d non-inverting input via R36, D4 and R35. This has the effect of a simulated high forward power voltage at the differential amplifier input. To ensure that this simulated voltage, which is constant, is not corrupted by any actual forward power dc voltage produced by the VSWR detectors, the junction of R38 and R39

is taken low by D6, which is biased on by the logic 0 at IC1b output. So under normal Rx conditions, ie with no reverse power dc voltage present, the output of the differential amplifier, IC2d is high, which produces a low output from IC2a. IC2a is connected to IC3c via R27, so IC3c output is at logic 1, which is then fed to IC3b whose other input, pin 5, is also at logic '1' via IC3d. Thus the set input to IC4a is at 0 under these conditions.

50 However, if there is a very large Rx signal, eg from a nearby transmitter, the reverse power dc voltage fed to IC2d rises and the output falls. When this output voltage falls below the threshold set by R30 the output from IC2a goes high, thus the SET input to IC4a changes to a logic 1, via IC3c and IC3b. IC4a (Q) output is connected to PL3-5, via R102, and when it is at logic 1 a Rx Protection signal is fed to Channelisation, which then generates alarm tones for the operator.

Tx PROTECTION

51 In the Tx mode the Tx/Rx select input is low, so TR8 is biased on via IC1b, the $\overline{Q}$ output from IC4a and IC11d. Under normal Tx conditions the Tx Protection input is low. This is fed to NAND gate IC3d, whose other input is high because of the forward power voltage present during transmission and fed to IC3d via R38 and D6. When Tx Protection goes high, the output from IC3d goes low and this sets the protection latch (IC4a). The $\overline{Q}$ output, now low, changes IC11d output to low, so turning TR8 off and setting RLA and RLB to the receive condition. The Q output, which is high, feeds a Tx Inhibit signal to Channelisation and this in turn produces an operator alarm tone.

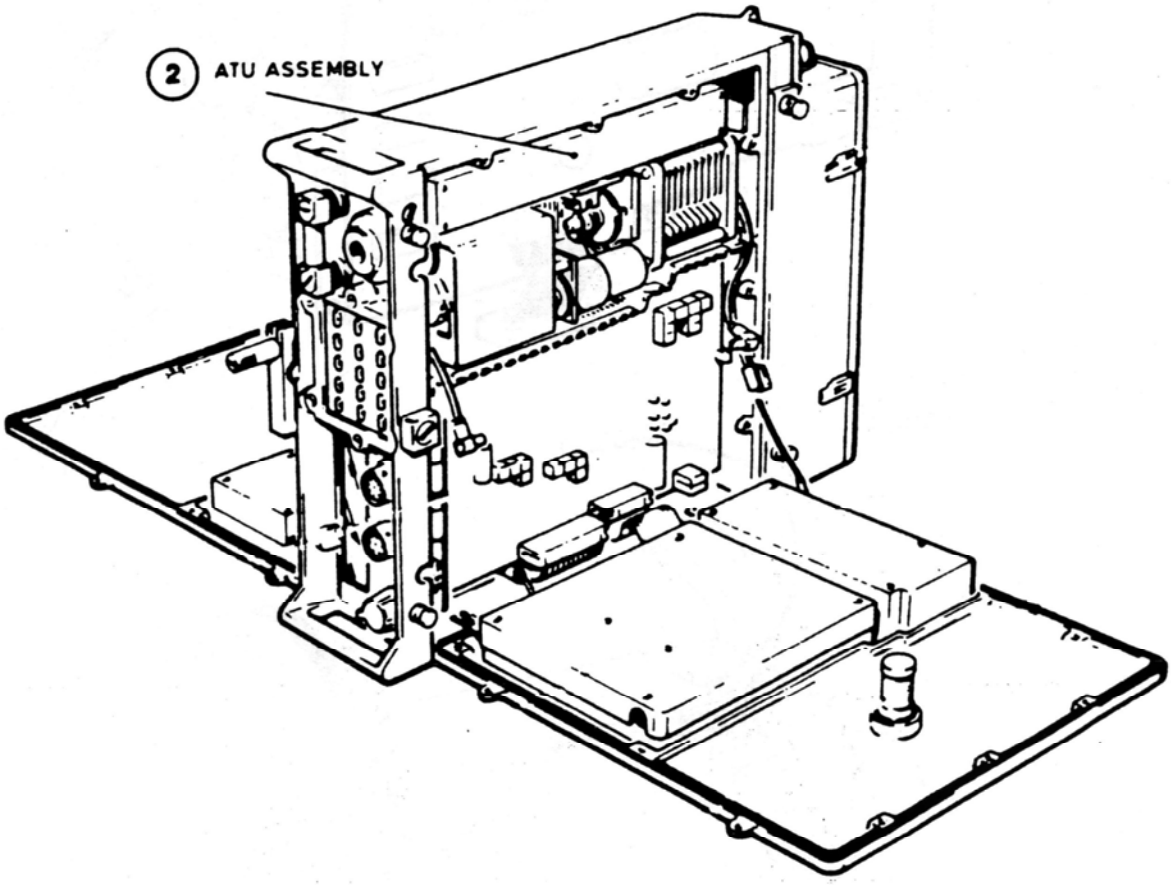


Fig 3.5.1 Antenna Tuning Unit Location

TP9608A4

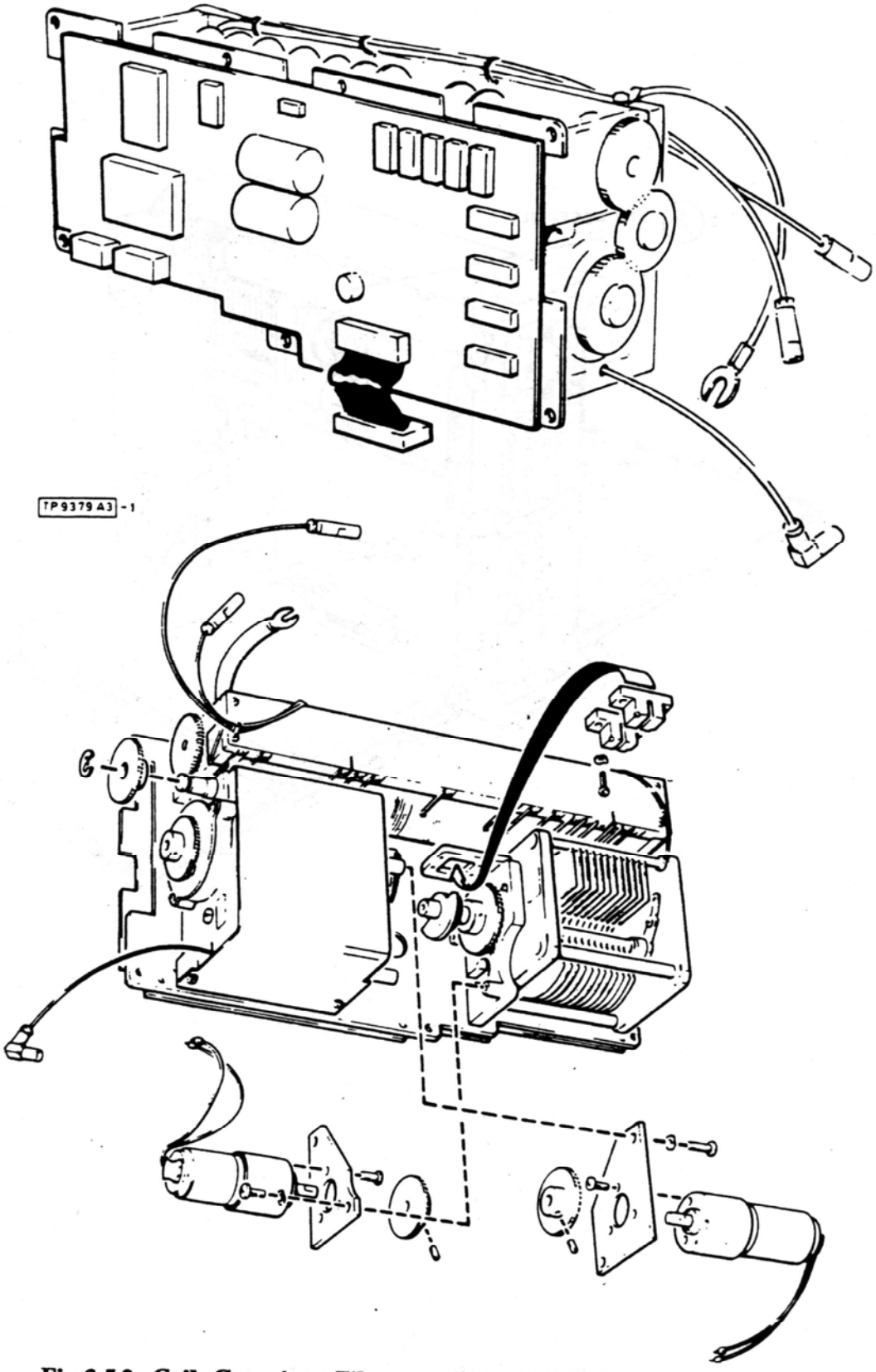


Fig 3.5.2 Coil, Capacitor, Filter and Control PEC Location

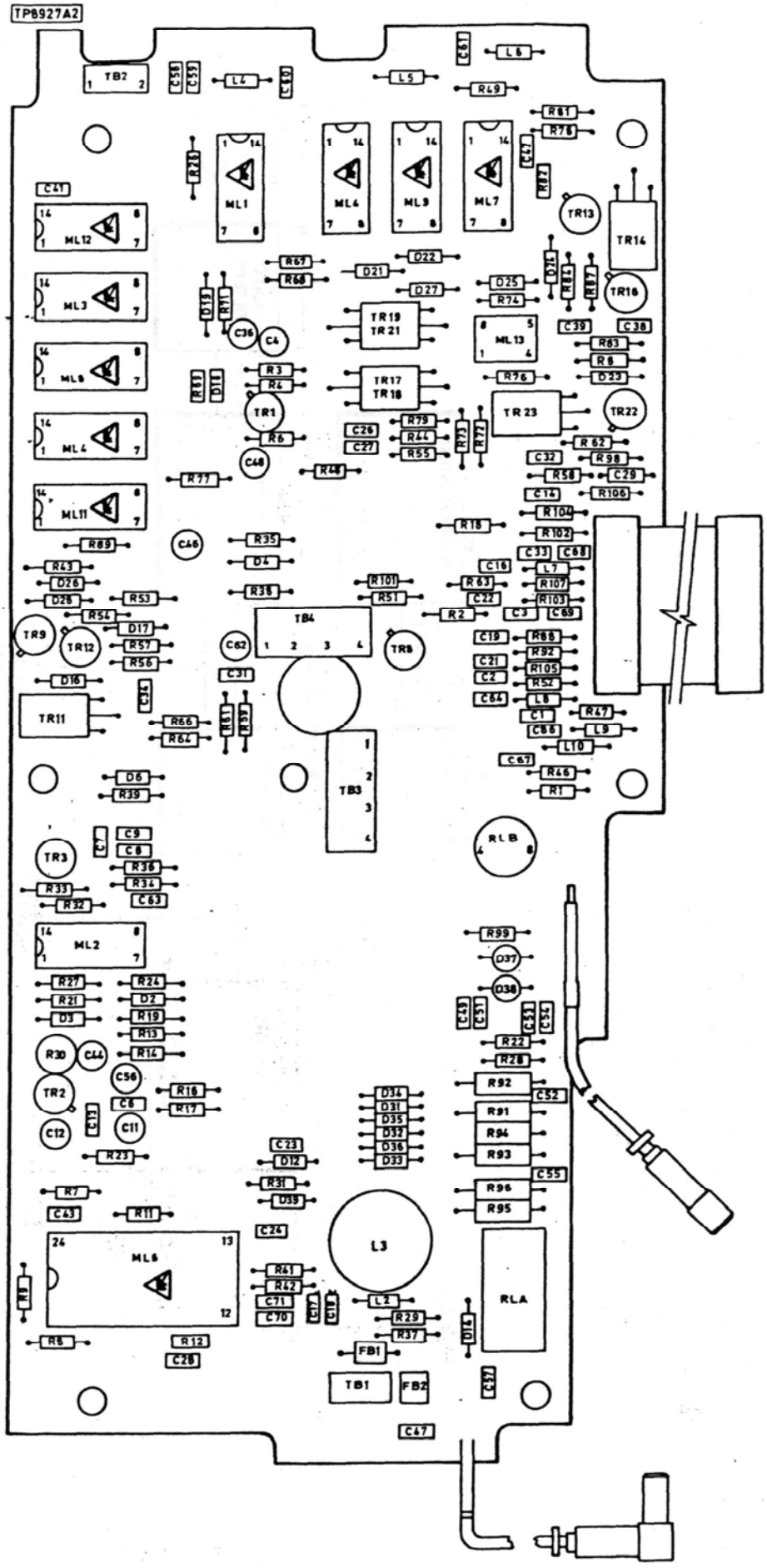


Fig 3.5.3 Control PEC Component Location

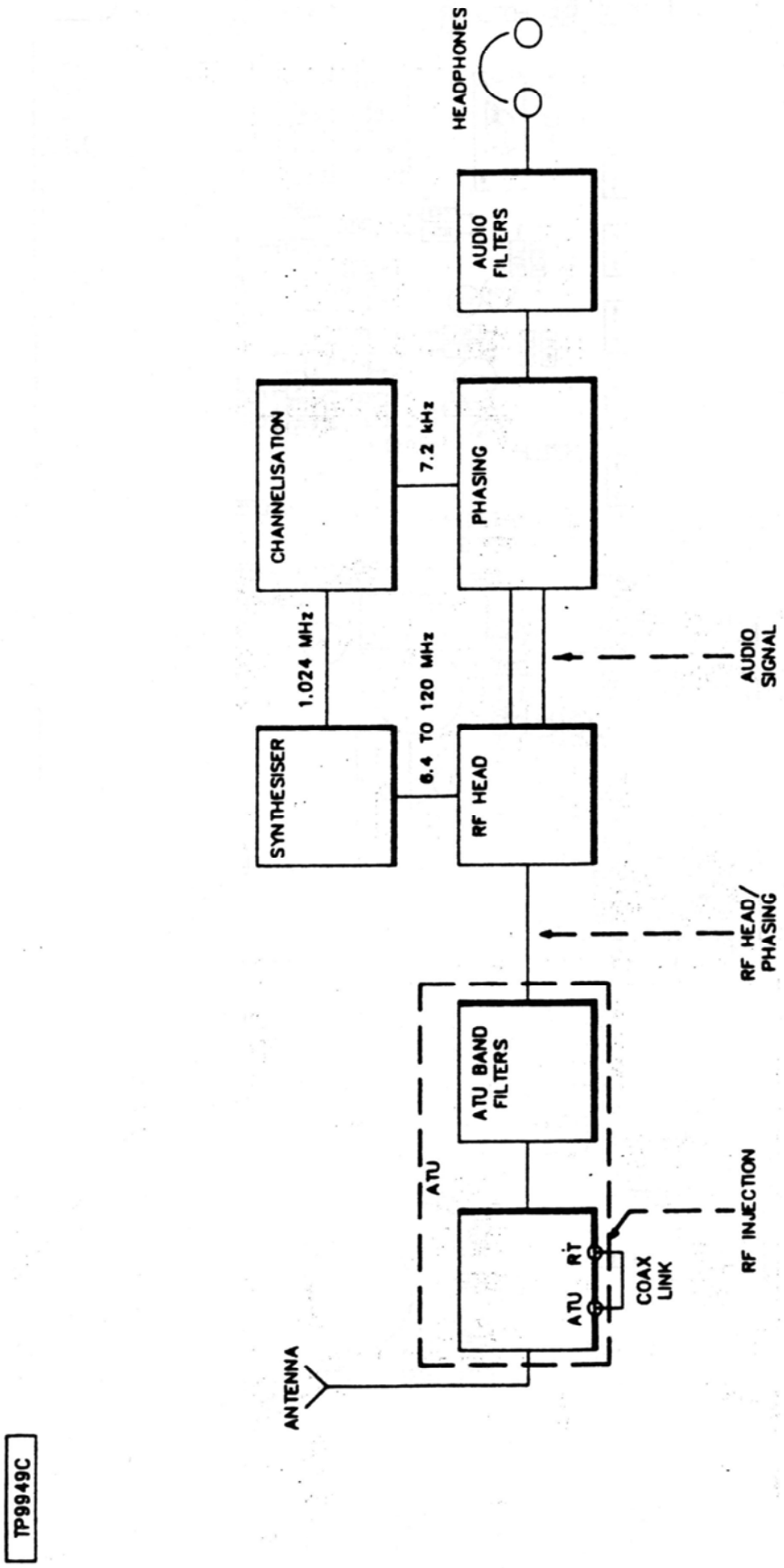


Fig 3.5.4 RF Signal Path (Receive)

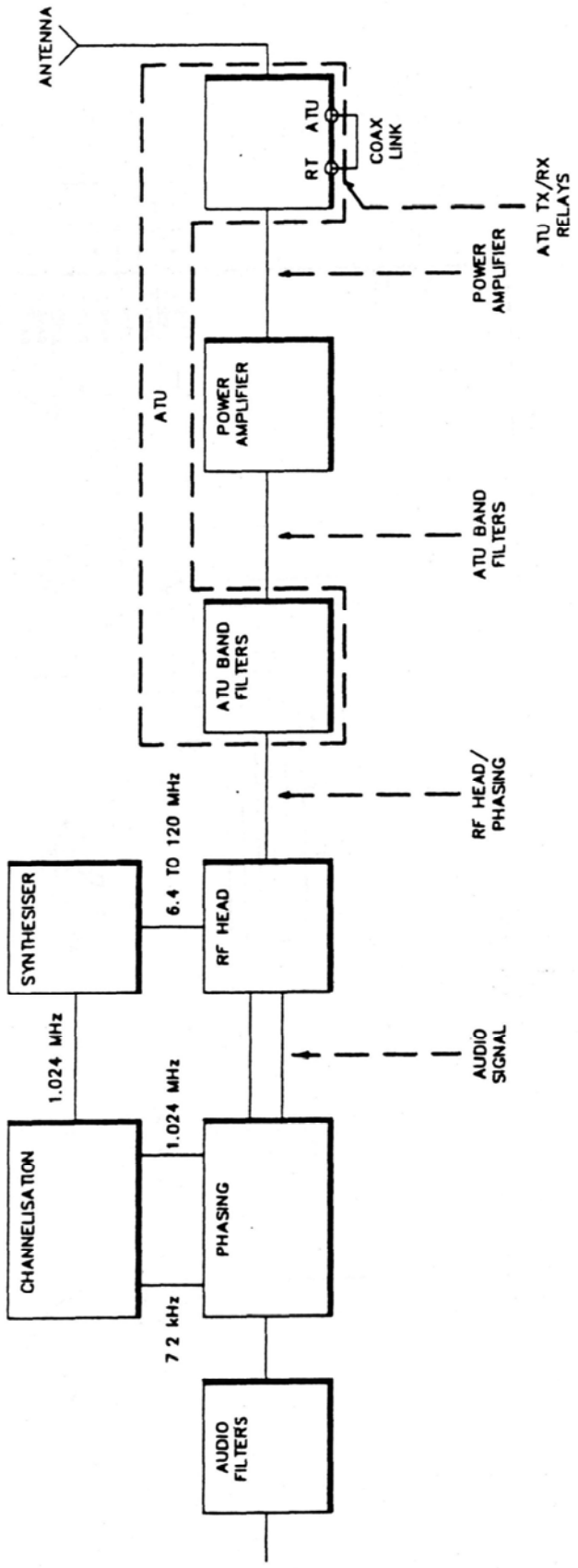


Fig 3.5.5 RF Signal Path (Transmit)

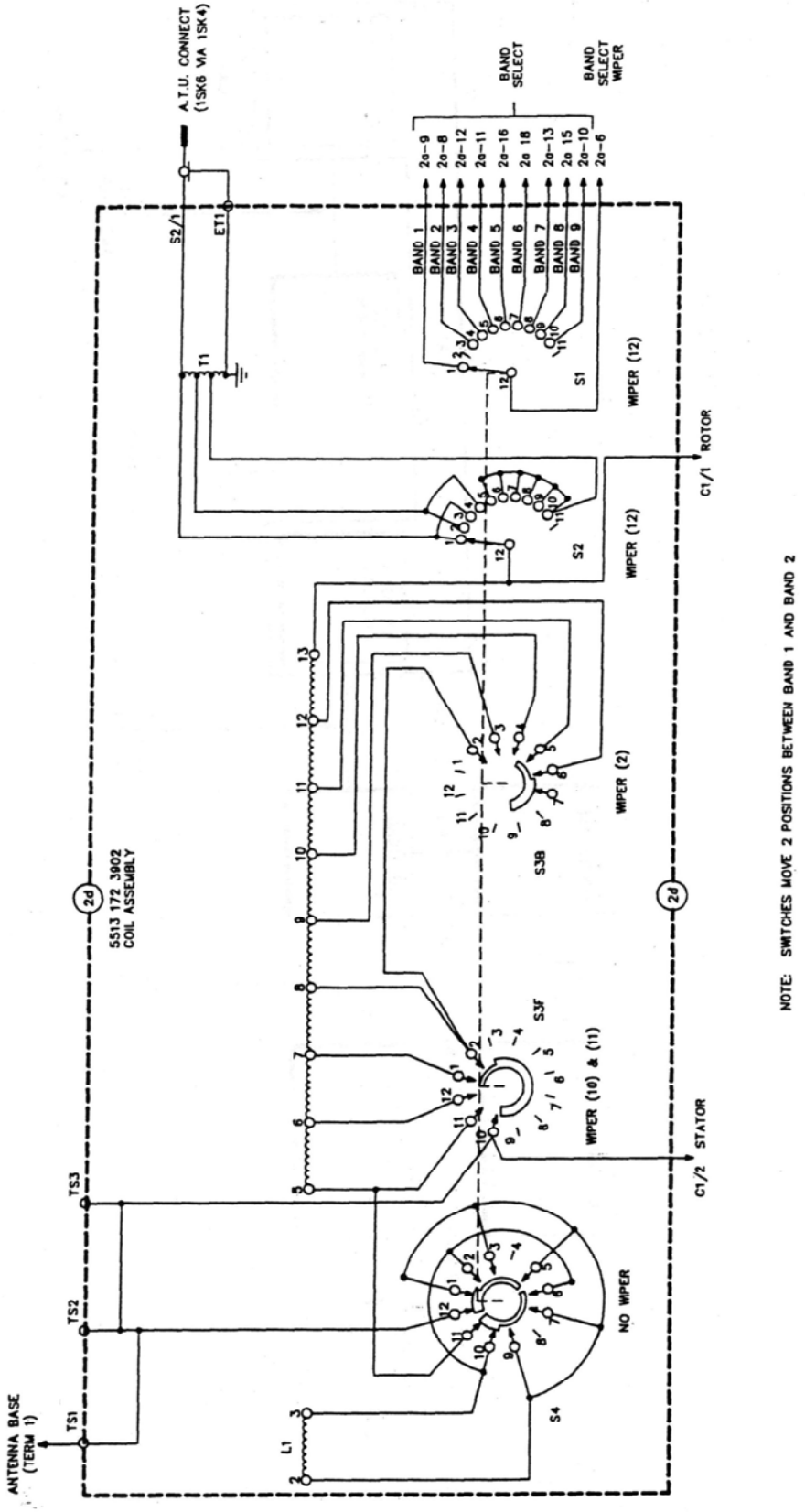


Fig 3.5.6 Coil Assembly Circuit Diagram

TP17830C

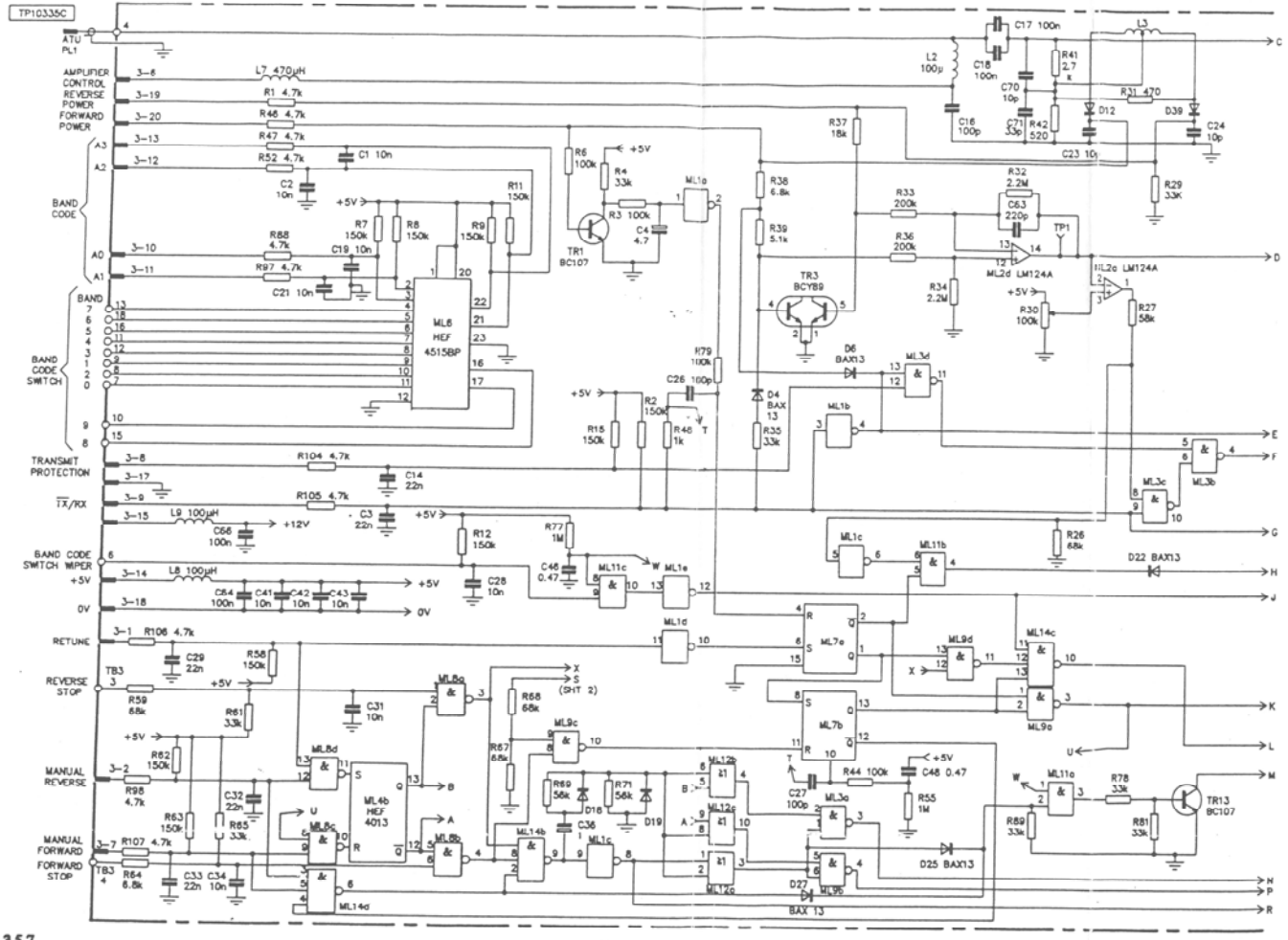


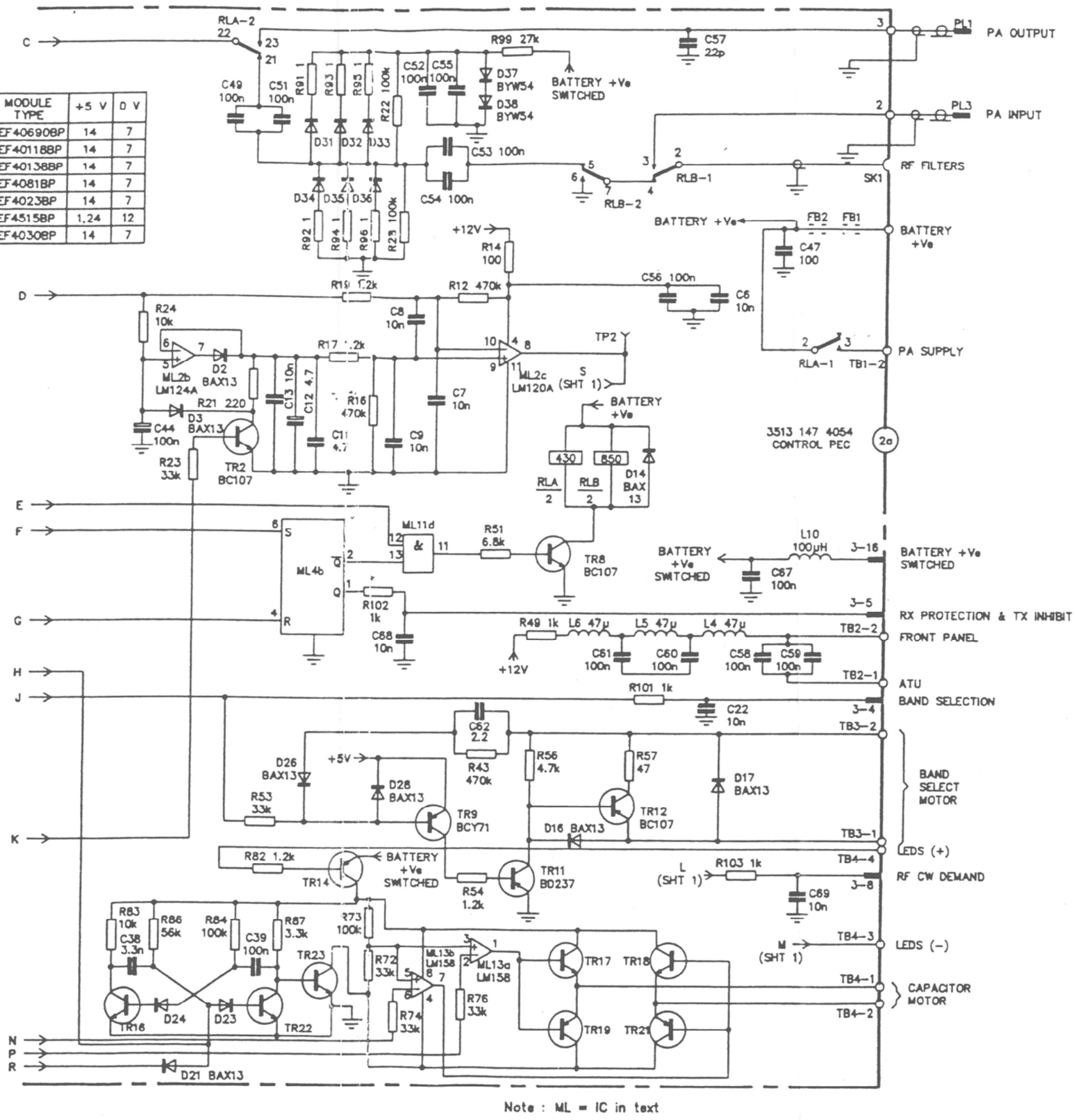
Fig 3.5.7

Control PEC Circuit Diagram (Sheet 1 of 2) Note : ML = IC in text

Fig 3.5.7

TP10347C

MODULE No	MODULE TYPE	+5 V	0 V
1	HEF40690BP	14	7
3,8,9	HEF40118BP	14	7
4,7	HEF40138BP	14	7
11	HEF4081BP	14	7
14	HEF4023BP	14	7
6	HEF4515BP	1,24	12
12	HEF40308P	14	7



Note : ML = IC in text

Fig 3.5.7 **Control PEC Circuit Diagram (Sheet 2 of 2)** **Fig 3.5.7**

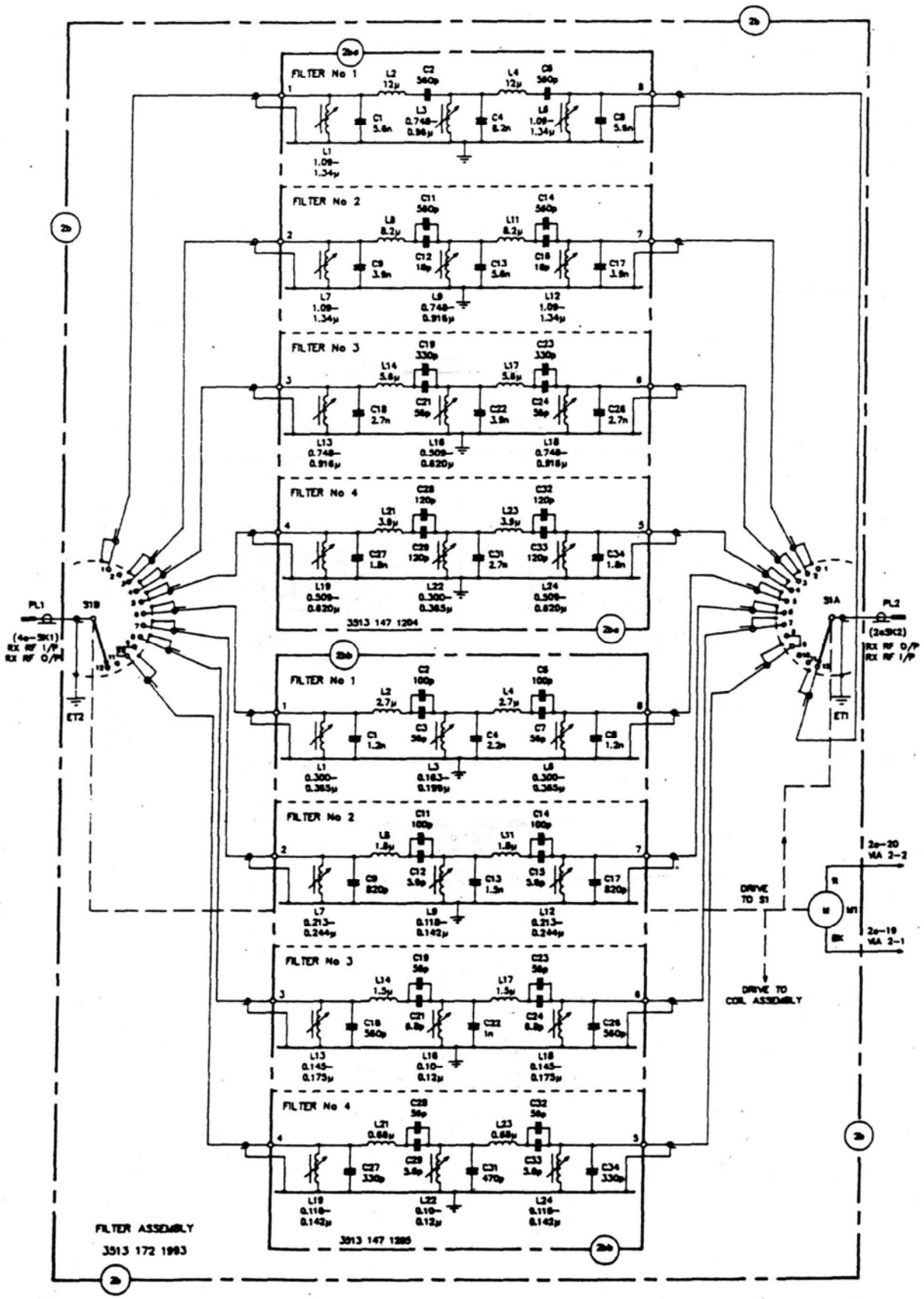


Fig 3.5.8 Filter Assembly Circuit Diagram

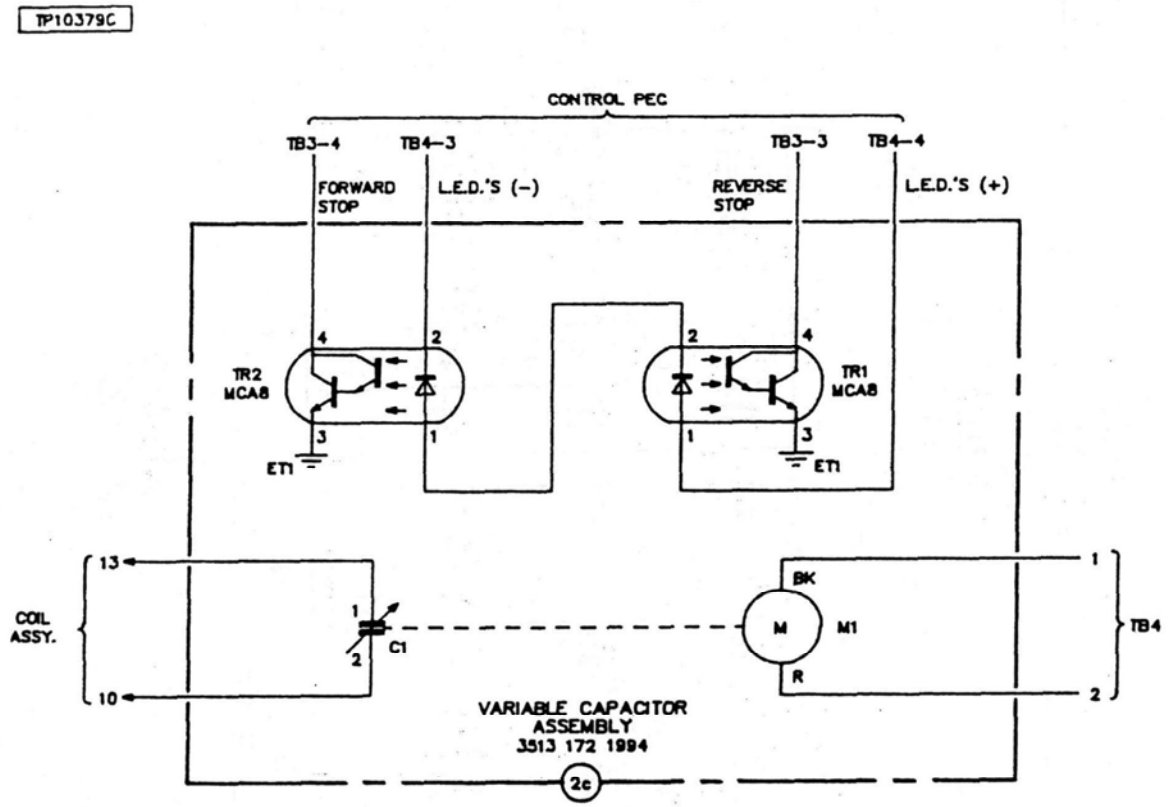


Fig 3.5.9 Variable Capacitor Assembly Circuit Diagram

CHAPTER 3.6

POWER SUPPLY UNIT

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CHAPTER 3.6

POWER SUPPLY UNIT

INTRODUCTION

1 The Power Supply Unit (PSU) converts the battery or external dc supply into other dc voltages used throughout the radio. The battery is located in a compartment at the back of the Callpac and connection is made via PL5 of the Case and Sub-unit Assembly. An external supply can also be connected to the Callpac via PL1 of the Case and Sub-unit Assembly. These supply voltages are the fed to the PSU via a protection PEC and the front panel rotary switch. These are also located on the Case and Sub-unit Assembly (see Cat 5, Fig 5.11).

2 The PSU itself forms part of the Upper Lid Assembly (Fig 3.6.1 - Item 3a) and consists of one PEC on which all of the circuitry is contained.

PROTECTION PEC

3 The protection PEC (Fig 3.6.4) provides reverse supply protection. The battery or external positive supply is fed to 1b-1 via a 5 amp fuse 1.FS1 and pin 2 of PL5. Reverse polarity protection is enabled by shunt diode D2. This diode conducts if the supply is connected in reverse and as there is little resistance on the line a large current flows causing the 5 amp fuse 1.FS1 to blow, thus protecting against reverse polarity.

4 The battery positive supply is fed from the protection PEC via a 1 amp fuse, 1b.FS1 and pin 4. A link from the front panel rotary switch (S1A), to pin 4 of the protection PEC is made on the PSU. When S1A is in any position other than OFF, the battery positive supply is switched to the PSU and is fed to TB3. The negative terminal of the battery is connected to the case and as an 0 V line to TB2 on the PSU sub-unit.

POWER SUPPLY UNIT

Input Filter

5 The input filter, comprising C3, L1 and C5, removes any ac component from the positive dc supply input; at the same time it prevents the pulsed voltage waveform, produced by TR1, being fed back down the positive dc supply line to the battery. The positive dc supply input is connected to TR1 emitter via L1 and a 1 amp fuse, 3a.F1.

Series Chopper

6 TR1 is a series chopper transistor, connected in series with the positive dc supply input. As the name implies it 'chops' the dc voltage present at its emitter terminal and produces a pulsed voltage waveform at its collector output. The pulsed voltage waveform produced by TR1 is, under normal operating conditions, approximately 15 V peak-to-peak at a frequency of 20 kHz and a mark-to-space ratio of 2:3. This is fed to the flyback circuit of L2, D1, C8 and C9 via T1 and T2 for conversion to a steady positive dc output (nominally +5 V). The switching of TR1, hence the pulse voltage waveform output, is controlled by TR2, which is connected to the base of TR1. When TR2 is on, the positive dc supply input is effectively connected to the base of TR1 biasing it off. Under normal operating conditions the switching of TR2 is controlled by the

voltage regulator (IC1), which is connected to TR2 base via pin 11, but TR2 can also be switched on by either the Standby signal applied to the PSU on P1-9, or under fault conditions by TR3 (see Standby Signal and Short Circuit Protection).

7 For more efficient operation of the PSU it is important that the pulsed voltage waveform, produced by the series chopper, has very fast rise and fall times. The 'switch-on' time of TR1 and hence the pulse rise time is improved by the action of T1. As TR1 turns on, the rising primary current in T1 induces a secondary voltage (windings 3-1, 2-8) whose polarity, after rectification by D3, turns TR1 on harder. This action reduces the switch-on time of TR1 and so gives a fast rise time of the pulsed voltage waveform. To prevent reverse voltage damage to TR1, D2 limits the maximum positive potential of T1 terminals 1 and 8 to 0.7 V above the +15 V dc supply input.

8 The switch-off time of TR1 and hence the pulse fall time is also improved by the action of T1. As TR2 turns on, TR1 turns off and T1 primary current falls rapidly. The resulting induced T1 secondary voltage has the opposite polarity to that at switch-on, so increasing the positive potential at TR1 and giving a more rapid turn-off. D3, ZD1 and also D2 ensure that a positive potential at TR1 base does not exceed the recommended reverse voltage for this device.

Standby Signal

9 P1-9 is the standby signal line from the special Control Handset, via Channelisation. When the operator selects 'STANDBY' this line is put low (0 V) and TR2 is switched on via base resistor R4. With TR2 on, the base potential of TR1 rises towards the dc supply input voltage on TB3, which biases TR1 off. All PSU output voltages are then zero and battery power is conserved.

Short Circuit Protection

10 The short-circuit protection network consists of transformer T2, base, bias resistor R2, decoupling capacitor C22 and switching transistor TR3. If the current drawn from the PSU is excessive the voltage induced into the secondary windings of T2, terminal 3-1 and 2-8, turns TR3 on, via base bias resistor R2. As the collector of TR3 is connected to TR2 base via R5, TR2 is also switched on, thus switching TR1 off. T2 secondary voltage then falls and TR3 turns off, thereby switching TR2 off, which allows the series chopper (TR1), to switch on again. The net result of this is that the pulsed voltage waveform produced by TR1 is greatly reduced in its average value and the dc output supplies of the PSU are reduced to a very small potential, thereby protecting the equipment.

Voltage Regulator (Fig 3.6.3)

11 Under normal operating conditions the voltage regulating circuit of IC1 controls the switching of TR2, whose base is connected to the collector of the output transistor of the IC via pin 11, and hence controls the switching of TR1. IC1 is a voltage regulator which, together with its external components, forms a positive switching regulator. The IC incorporates a temperature compensated reference amplifier, an error amplifier, an output transistor and a current limiter.

12 The reference amplifier supplies a reference voltage to the inverting input of the error amplifier. This reference voltage is divided by the potential divider network R7 and R8 to give approximately +5 V at pin 4 of the IC; this is ac decoupled by C10. The reference voltage is

also fed to the base of the current limiter (IC1 pin 2) which has its emitter connected to the +5 V dc supply (IC1 pin 3) thus preventing over-driving of the output transistor. Also fed to this point, ie IC1 pins 2 and 4, is a synchronising signal generated by the oscillator in the dc-to-dc converter, via C23 and R13. (See para 19 for explanation of synchronisation.)

13 The non-inverting input of the error amplifier (IC1 pin 5), is fed via R9 with a sample of the steady dc voltage produced by the flyback circuit. R9 is rf decoupled by C7. The error amplifier provides base bias for the output transistor, which is dependent upon the difference between the divided-down reference voltage and the fed back sample voltage (nominally +5 V). The reference and error amplifier within IC1 have Vcc of +15 V fed in from the PSU dc input supply via pin 12.

14 The output transistor of IC1 has as its emitter resistor R6, which is connected between pin 10 and the +5 V sample fed back from L2 thereby regulating the switching of TR1. The IC output transistor controls the switching of TR2, thereby regulating the switching of TR1. When the sample voltage at pin 5 exceeds the reference voltage at pin 4 the error amplifier switches the output transistor on. This turns TR2 on and so applies +15 V to the base of TR1, turning it off. Thus the switching of TR1, and therefore the mark/space ratio of the pulsed voltage waveform, is controlled by the +5 V sample. A synchronising signal, from the dc-to-dc converter, is also fed to the voltage regulator. This signal is connected to IC1 pin 4, the inverting input of the error amplifier. When this voltage is above the sample voltage present on pin 5 the output transistor of IC1 is turned off. Hence TR2 also is turned off and TR1 is switched on. The synchronising signal is at the same frequency as that of the free-running oscillator contained within the dc-to-dc converter. As this is approximately 20 kHz then every 50 µsec the synchronising signal voltage fed to IC1 pin 4 is greater than the sample voltage on pin 5. Therefore, TR1 is switched on every 50 µseconds (see para 19 for explanation of synchronising signal).

Flyback Circuit (Fig 3.6.5)

15 The flyback circuit, which consists of D1, T1, T2, L2, C8, C9, C24 and R14, is a type of discharge circuit that by its action produces a steady dc voltage output (nominally +5 V) from the pulsed voltage waveform produced by TR1. With TR1 switched on C9 charges up via L2. When TR1 switches off C9 discharges via the output dc supplies. The field in L2 then collapses, producing a back emf that makes D1 cathode more negative than its anode thus biasing it on. This maintains the current through the choke L2, hence maintaining the current being drawn from the PSU along the dc output supply lines. The energy stored in L2 is transferred to the positive plate of C9 by this same current, resulting in a steady dc voltage at this point. This voltage is then fed to:

(a) the Voltage Regulator, IC1

(b) the DC-to-DC Converter TR4, TR5, T4 etc.

(c) the +5 V Output Filter and Over-voltage Protection Circuit of D2, L3 etc.

16 The steady dc voltage produced by the flyback circuit is nominally +5 V, but this value is dependent upon the mark-to-space ratio of the pulsed voltage waveform produced by TR1. Under normal operation the mark-to-space ratio is approximately 2:3, which the flyback circuit converts to +5 V dc. If the voltage produced by the flyback circuit is above this nominal value then the sample voltage fed back to IC1 is also high (relative to the normal). This results in TR1

being switched off earlier than usual, hence the 'on' time (ie the mark time) of the pulsed voltage waveform is reduced and so the steady dc voltage produced by the flyback circuit falls. When TR1 switches back on again D1 cannot switch off immediately, so R14 and C24 are connected across D1 to the 0 V line to remove any spikes that might otherwise appear on the dc output line.

DC-to-DC Converter (Fig 3.6.5)

17 The steady dc voltage produced by the flyback circuit is fed to the centre tap of T4 and R11 for conversion to the other output dc supplies, and C12/C13 provide rf decoupling at this point. Base bias for TR4 and TR5 is provided by R11. Suppose that TR5 switches on first, then a collector current flows via T4 centre-tap (terminal 8), through the winding of T4 to terminal 7, then through T3 terminals 7 and 6 to TR5. The phase relationships of T3 windings are such that when this current is flowing the voltage induced into T3 winding 1 and 3 biases TR5 on and the voltage induced into T3 winding 2 and 8 biases TR4 off. As the current through T3 increases the transformer will reach saturation so the induced voltage fed to TR4 and TR5 base will level off, leading to a fall in current through the transformer. At this point the magnetic field of T3 collapses and thereby induces voltages of opposite polarity into the windings, hence TR5 is switched off and TR4 is switched on. The cycle keeps repeating and the circuit oscillates at approximately 20 kHz. The bases of TR4 and TR5 are ac decoupled by C25 and are protected against reverse bias breakdown by D4, which limits the negative voltage applied to the transistor bases.

18 T4 is an auto-transformer with six windings on the same core; four of the windings, terminal 1, 2, 6, 7 and 8 have +5 V connected to the centre-tap, which supplies the energy to run the oscillatory circuit of TR4 and TR5. The other windings, terminals 3, 4 and 5 have a centre-tap referenced to the 0 V line; consider these two windings first. When the oscillator is running a voltage is induced into T4 and, say, terminal 3 goes positive with respect to the centre-tap, then terminal 5 is negative so D5 is biased on, thus driving current through the load connected to P1-1 and P1-2. When the voltage at terminal 3 goes negative, the voltage at terminal 5 is positive, thus forward biasing D6. The turns ratio of this part of T4 is such that +6 V dc is produced by D5 and D6. D7 and D8 function in the same way to produce a -6 V dc voltage. The phase relation of the windings of T4 is such that a voltage induced in winding 6 and 7 adds to the voltage in winding 7 and 8; similarly, a voltage induced in winding 1 and 2 adds to the voltage in winding 8 and 1. D9 conducts when T4 terminal 6 is positive with respect to the centre-tap and D10 conducts when T4 terminal 2 is positive with respect to the centre-tap, thus producing a +12 V dc output.

Synchronisation

19 To reduce the level of noise on the dc output supply lines of the PSU, TR1 is synchronised to switch at the same frequency as the oscillator in the dc to dc converter. This is done connecting TR4 collector via R13 and C23 to IC1 pin 4, which is the reference voltage input to the error amplifier. When TR4 switches off, the voltage at its collector rises towards +5 V, so making the reference voltage input of the error amp (IC1/4) appear higher than the sample voltage input (IC1/5). Thus the error amplifier switches the output transistor of IC1 off, which turns TR2 off and TR1 on, thereby synchronising the switching of TR1.

FILTERS AND OVER-VOLTAGE PROTECTION

20 All the dc output supply lines pass through dc smoothing circuits to remove any ac ripple, also each supply is protected against over-voltage.

(a) The +5 V dc output is smoothed by rf choke L3, smoothing capacitor C15 and reservoir capacitor C14. ZD2 is a 6.2 V zener diode connected between the +5 V supply line and the 0 V rail for over-voltage protection. The +5 V dc output is fed from the PSU on P1-5 and P1-6.

(b) Smoothing of the +6 V dc output is done by rf choke L4, smoothing capacitor C17 and reservoir capacitor C16. Over-voltage protection is provided by ZD3, a 6.8 V zener diode. The +6 V dc supply is output from the PSU on P1-1. A separate connection is made from the +6 V dc supply to provide +6 V for the AGC; this voltage is output on P1-2 with connection to the 0 V reference being made on P1-3.

(c) The -6 V dc output supply is smoothed by rf choke L5, smoothing capacitor C19 and reservoir capacitor C18. Another 6.8 V zener diode, ZD4, provides over-voltage protection for this supply which is fed out of the PSU on P1-7.

(d) Smoothing of the +12 V dc output supply is done by rf choke L6, smoothing capacitor C21 and reservoir capacitor C20. Over-voltage protection is provided by ZD5, a 13 V zener diode. The +12 V is output from the PSU on P1-8.

INTERCONNECTIONS

21 The PSU has several terminals that provide interconnections for ancillary and optional equipments used with the Callpac (eg Battery Charger); these interconnections have no effect upon the operation of the PSU and are:

(a)	LP Selection External	-	P1-10 to TB1
(b)	Battery Positive Supply	-	TB4 to TB6
(c)	External DC Supply	-	TB5 to TB7

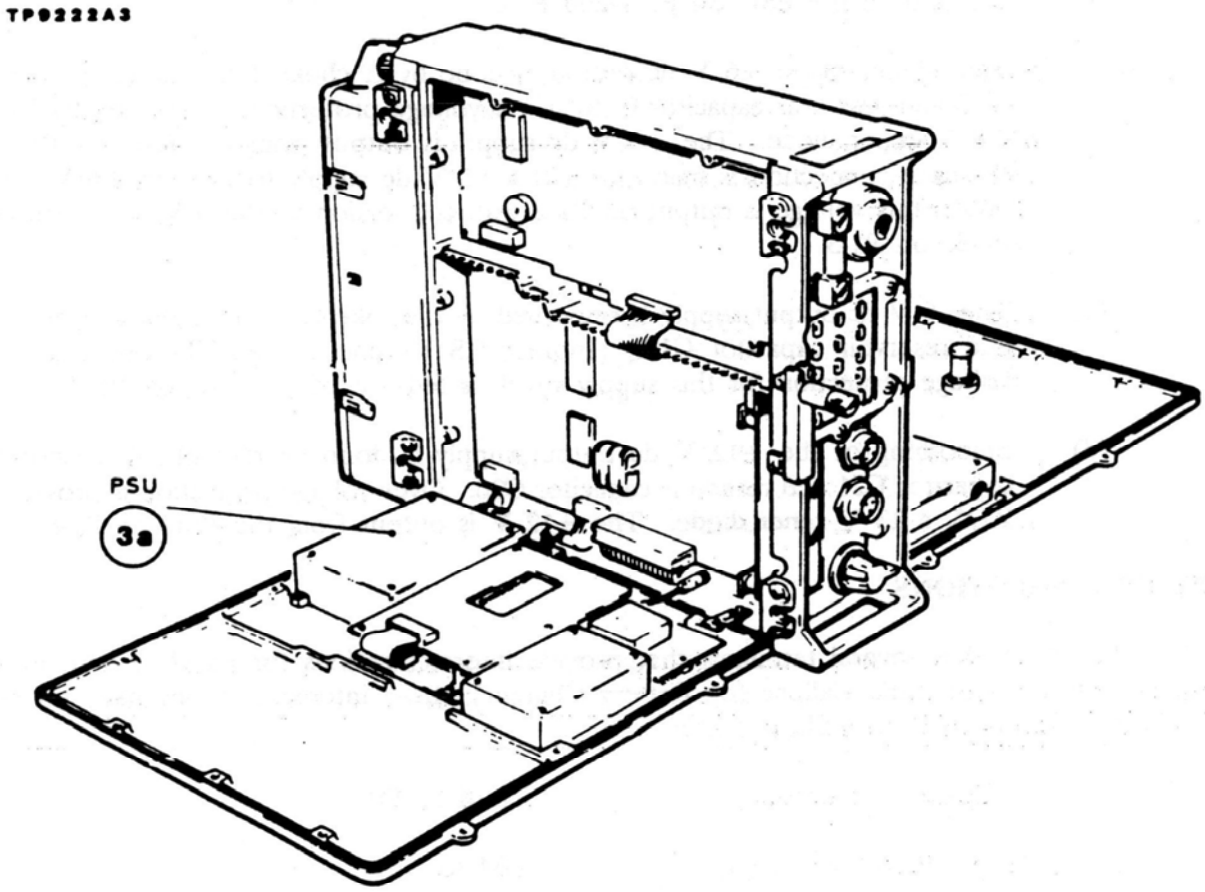


Fig 3.6.1 Power Supply Unit Location

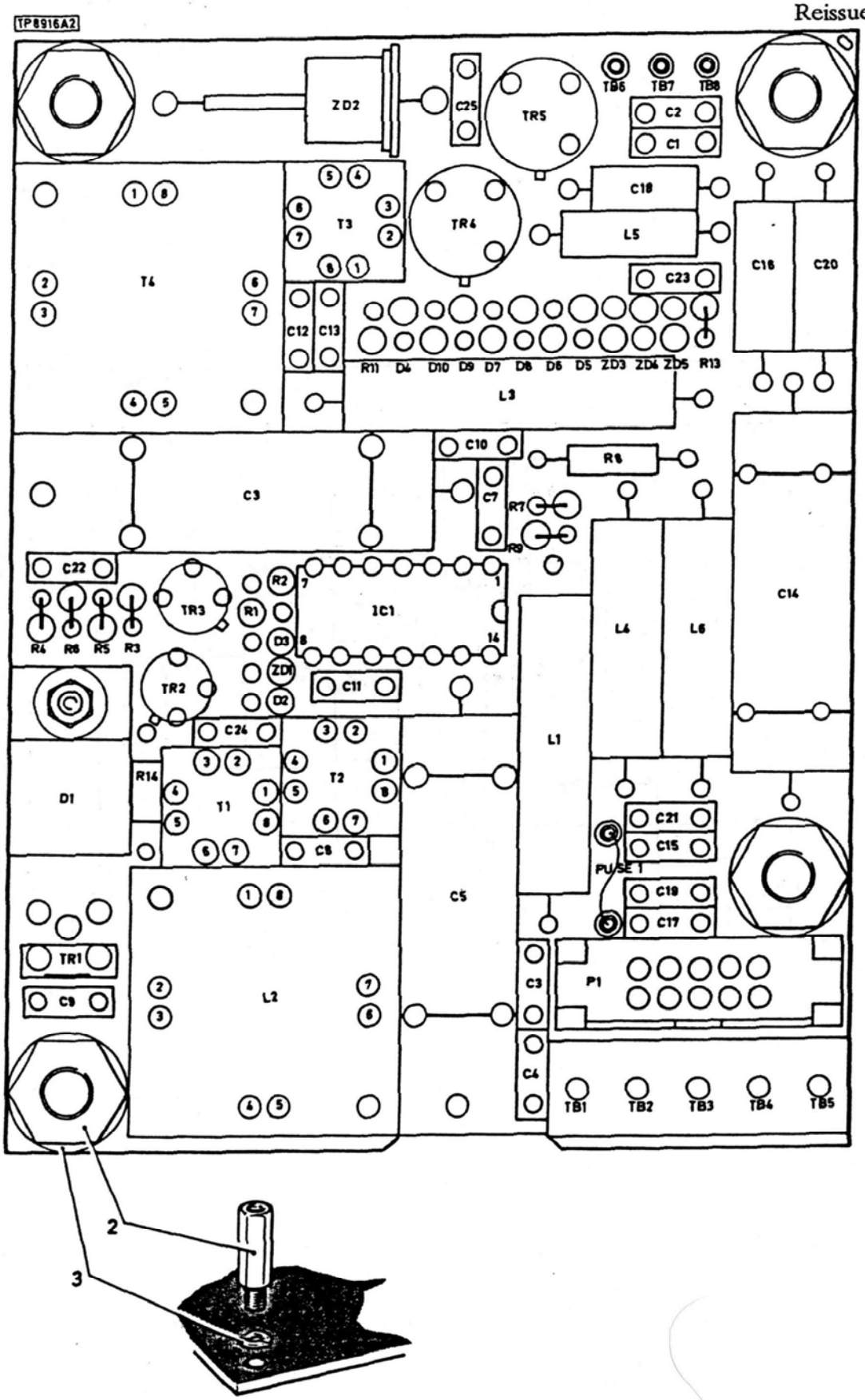


Fig 3.6.2 Power Supply Unit Component Location

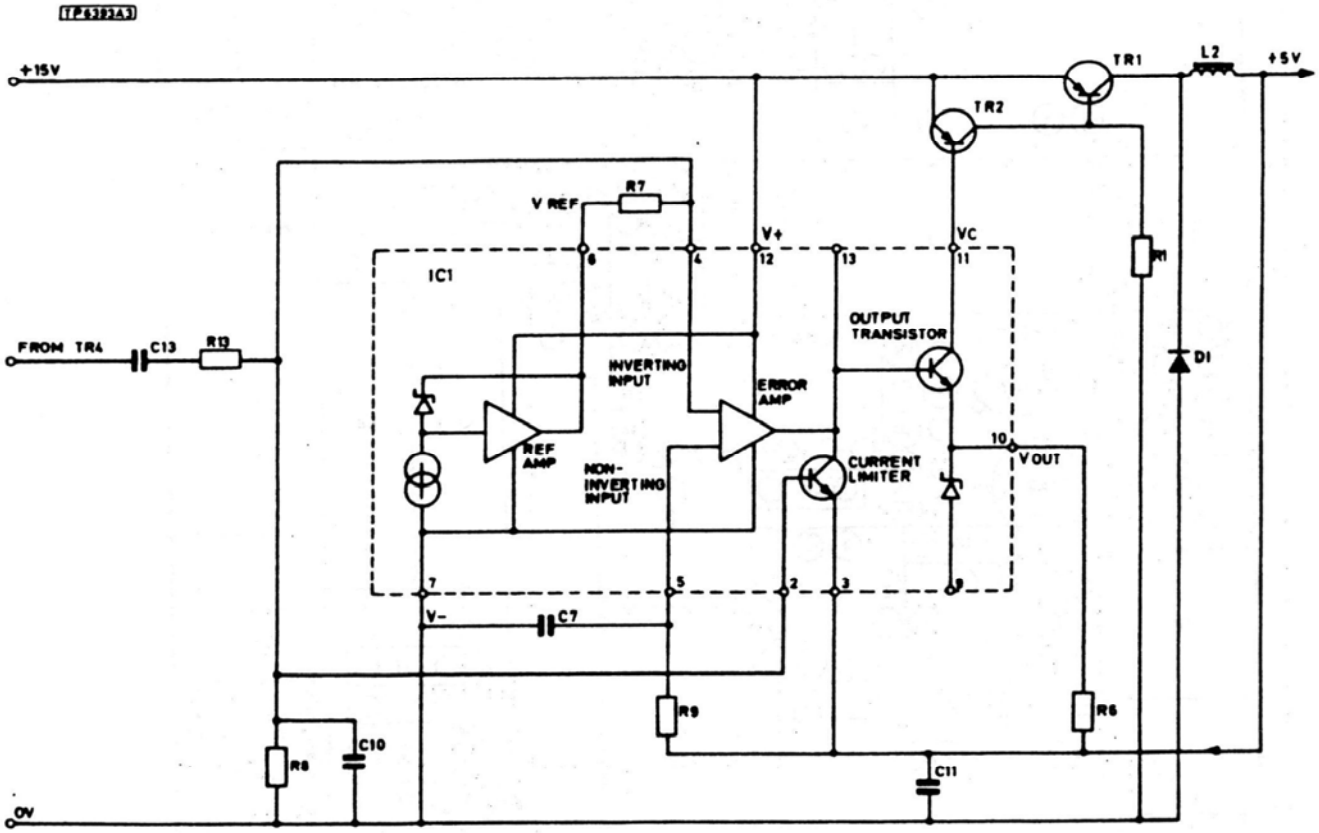
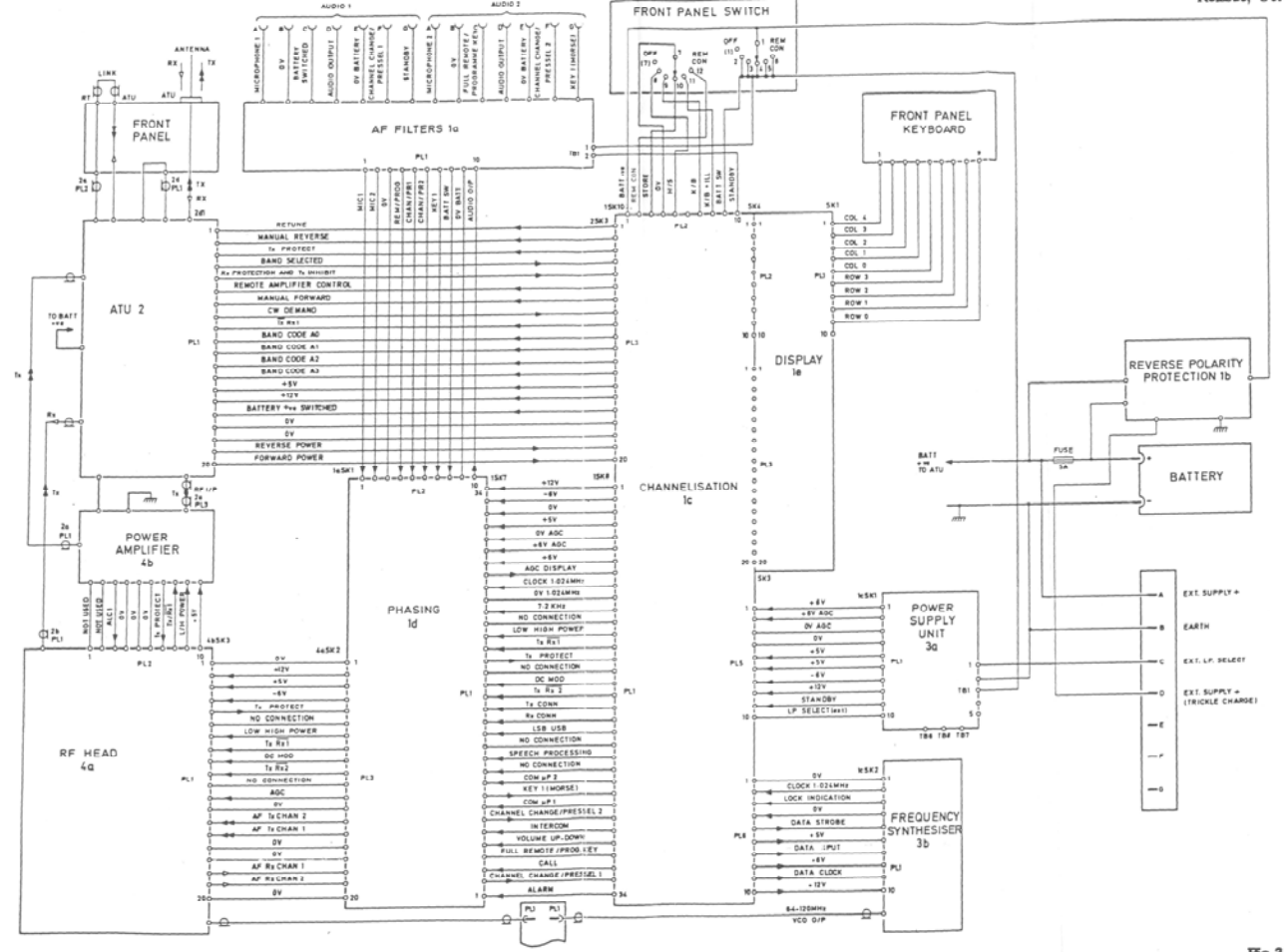


Fig 3.6.3 Voltage Regulator IC : Schematic Diagram



Protection PEC Circuit and Interconnection Diagram

Fig 3.6.4

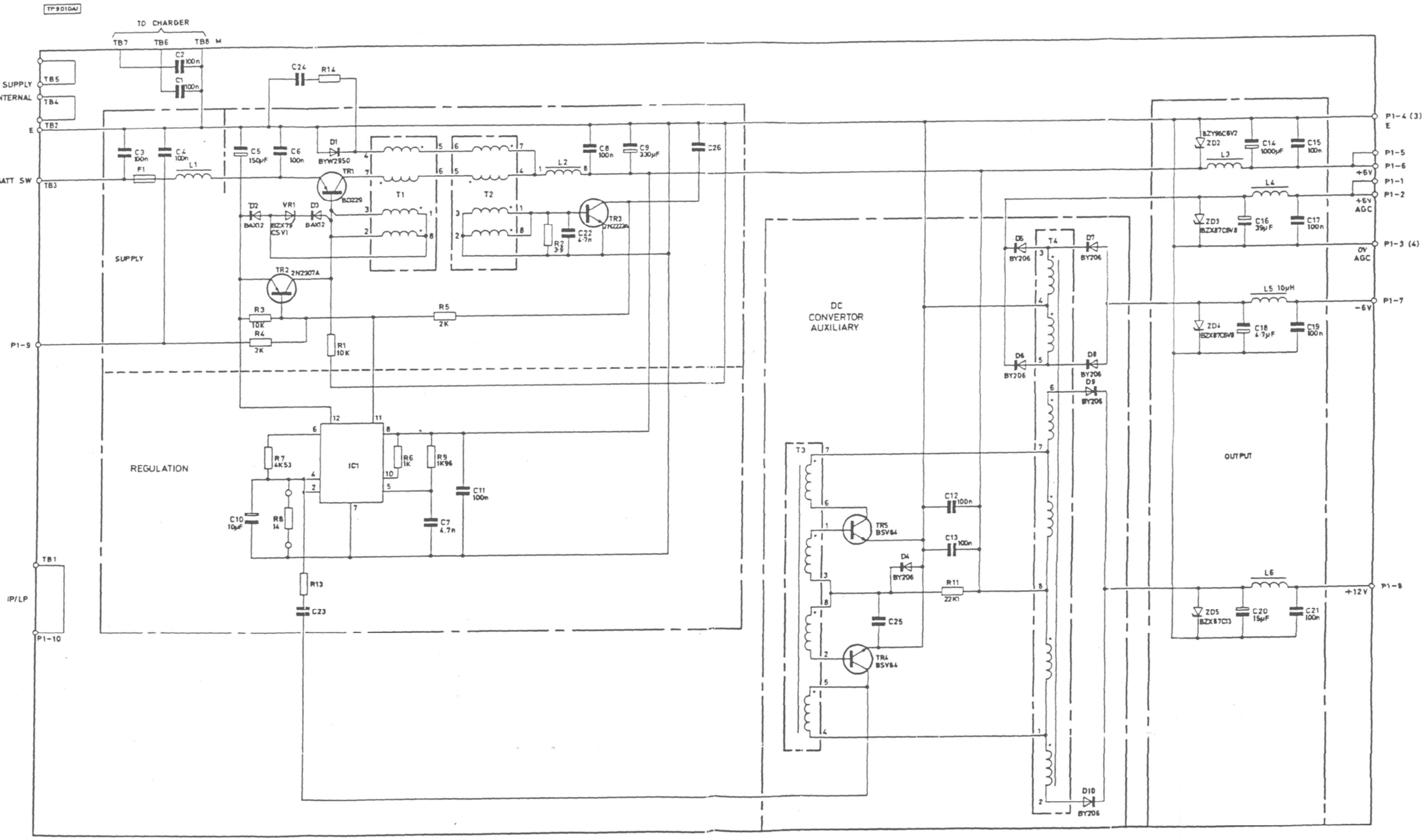


Fig 3.6.5 Power Supply Unit Circuit Diagram Fig 3.6.5

CHAPTER 3.7

POWER AMPLIFIER

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CHAPTER 3.7

POWER AMPLIFIER

INTRODUCTION

1 The Power Amplifier (PA) (Fig 3.7.1) forms part of the Lower Lid Assembly (See Chap 3.0, Fig 3.0.1 - Item 4ba) and consists of one PEC (Fig 3.7.2) on which all of the circuitry is contained.

DRIVER STAGE (Fig 3.7.3)

2 The rf signal from the RF Head is input to the power amplifier on J1, via the filter assembly. This input is transformer coupled by T1 to the driver stage, which is a normal class AB push-pull amplifier. The two driver transistors, TR9 and TR10, are a matched pair of high power gain transistors, whose collector load is T2, which couples the driver stage to the power output stage. R30/C12 and R31/C13 provide negative feedback to control the gain of both transistors, and rf decoupling for the stage is by capacitors C14, C15, C18 and C28. The centre-tap of the primary of T2 is taken to +15 V and C17, which is across the primary of T2, provides high frequency compensation and impedance matching for the transformer.

Driver Bias

3 Biasing for the drivers is supplied by TR14 and TR15, and is applied to TR9 and TR10 bases via the centre tap of T1 secondary. Bias is adjusted by R43 in the quiescent steady state to give correct collector current of TR9 and TR10, ie 22 mA. Thermal compensation of the bias supply is obtained by mounting TR14 on the same heatsink as the driver transistors. Any increase in temperature, after the bias had been correctly adjusted, causes TR14 to conduct more so the voltage at TR15 base falls, causing a decrease in bias at the bases of TR9 and TR10. This in turn produces a drop in temperature of TR14 and thermal balance is restored.

POWER OUTPUT STAGE (Fig 3.7.3)

4 The power output stage is similar to the driver stage in that it is a class AB push-pull amplifier, having transformer coupling at its input and output. The driver output is coupled to the output stage by T2 and the rf signal is fed to the bases of TR11 and TR12, a pair of matched power transistors, whose collector load is T3, whilst C19, C22, C23, C26 and C27 are all decoupling capacitors. Input impedance matching is provided by R34, R35, R36, R37, C20 and C21 and the chokes L3, L4, L5 and L6 isolate the rf at the bases from the bias supply. The amplified rf signal is transformer coupled to the output by T3, which has its primary centre tap taken to +15 V, and the amplified rf output is then fed back into the ATU, via J2.

Power Output Stage Bias

5 Biasing for the power output transistors is provided by TR16 and TR17, and is applied to the bases of TR11 and TR12 via L5 and L6. The bias is adjusted by R48 to give a quiescent collector current of 120 mA in total. The bias circuitry is almost identical to that for the drivers, with thermal compensation provided by TR16 being on the same heatsink as TR11 and TR12.

TR17 is a Darlington pair transistor to give the high current gain necessary to supply the bias for the power output transistors, which have their bases rf decoupled by C30 and C31.

OUTPUT POWER LEVEL AND ALC (Fig 3.7.3)

6 The power amplifier provides two levels of output power both of which are controlled by an Automatic Level Control (ALC) system. Switching from one power level to the other, and ALC at either level, are performed by interlinked circuits. The ALC circuit provided a varying voltage that is used for gain control in the RF Head (see Chap 3.3). After power amplification, the rf output drives a pair of peak detecting diodes whose standing dc bias is switched to provide the low power or high power outputs. Before considering how the peak detector diodes control the power output level, it is necessary to know how their standing bias is derived from the two required output levels.

Peak Detector Bias

7 The peak detecting diodes are D3 and D5, and their standing dc bias is the voltage developed across R40. How this is so is better appreciated by noting that at dc the resistors R24, R25 and R28 are virtually short-circuited by T4 and T5 so that the anodes of D3 and D5 can be considered as being connected together to the top end of R40.

8 In the transmit mode the battery voltage is applied to the constant current generator comprising T6, ZD3 and R18, which supplies a constant current through ZD4. Thus the potential at the top of R20 is +5 V (supply) plus 2.1 V, ie 7.1 V. In the low power mode, TR8 is off and R20 is adjusted to give a peak detector bias of approximately 5.4 V, which corresponds to the nominal low power output of 4 W.

9 When the high power mode is selected, the logic level at J3/9 (Low/High Power) is low, which, after inversion by IC2, turns TR8 on and connects R21, R22 in parallel with R40. The peak detector bias is therefore reduced to approximately 4 V, the actual value being set by R22 to give the nominal high power output of 20 W.

Peak Detector Operation.

10 The rf output power from T3 secondary is connected to a peak current transformer T4 and a peak voltage transformer T5. Since T4 is current driven and T5 is voltage driven, the phase difference between their output voltage peaks gives a smoother base drive voltage for TR5 that is still proportional to the rf output from T3. Until the rf output produces voltage peaks in excess of the bias developed across R40 then TR5 remains off. When the peaks exceed the bias, D3 and D5 provide a base current that turns TR5 on.

11 In the low power mode the standing bias is such that D3 and D5 are not conducting so a small voltage from T4 and T5 is sufficient to turn them on. In the high power mode the standing bias is lower and consequently a higher rf output is necessary before D3 and D5 become conducting. Correct rf loading of T4 and T5 is provided by R24/R25 and R28 respectively; C11 provides frequency compensation for the peak detectors.

Automatic Level Control (ALC)

12 The ALC circuit comprises TR5, TR3 and the field-effect transistor (FET)-TR2. When TR5 is on, TR3 is turned on and this supplies a gate voltage for TR2 via D2. TR2 is a low-

impedance source follower output stage for the ALC control voltage fed out via divider R7/R8 as ALC1 (the other output at ALC2 is connected to 0 V and is not used). A rise in peak value of the rf causes TR5 to be turned on harder, so increasing the ALC output voltage; a fall in rf output results in a corresponding fall in ALC voltage.

13 As in an AGC system, rapid increases in power must be compensated quickly, while a reduction in output power is compensated more slowly, and this is achieved by the peak holding circuit of D2, R12, C6 and R11. For example, if the rf output power increases sharply then D3 and D5 turn TR5 on harder and TR3 also is turned on harder; the voltage at the junction of D2/R12 increases, and C6 charges quickly via R12, with a time constant:

$$t = C \times R = C6 \times R12$$
$$= 220\ nF \times 162\ ohms$$
$$= 35\ \mu secs$$

14 If the rf output power is reduced, causing the voltage at D2 cathode to fall, then C6 discharges via R12 and R11 (as R11 is a much greater value than R12, R12 can be ignored) in a time constant:

$$t = C \times R = C6 \times R11$$
$$= 220\ nF \times 10\ Megohms$$
$$= 2.2\ seconds$$

Thus the peak ALC voltage stored by C6 maintains the high level of ALC controlling voltage if the rf output power falls, thereby stabilising the control loop.

Thermal ALC

15 As well as bias temperature compensation of the power output stage (para 3) the PA also incorporates a thermal ALC circuit for further protection of the transmitter against over temperature. The thermal ALC circuit, switched on by TR13 (see para 20), consists of TR18, with base bias resistors R52 and R53, base rf decoupler C3 and emitter resistor R54. R53 is a thermistor mounted on the same heatsink as the power output stage transistors (TR11 and TR12); when the temperature of this stage increases, the resistance of R53 increases so raising the base voltage of TR18. At some point TR18 is turned on, so increasing the base current of TR3, whose collector potential then rises. This increases the ALC controlling voltage (which is fed to the RF Amp in the RF Head), so reducing the rf signal fed to the power output stage, which in turn reduces the temperature of this stage.

PROTECTION CIRCUITS (Fig 3.7.3)

16 The PA has two protection circuits:

(a) Overdrive Protection

(b) Transmitter Protection

Overdrive Protection

17 Overdrive protection is provided to prevent the PA power output stage transistors (TR11 and TR12), from bottoming and thereby producing gross distortion of the rf output waveform.

The circuit consists of clamping diodes D6 and D7, which clamp the emitter of TR4 to the collectors of TR11 and TR12. The base bias voltage for TR4 is derived from the peak detector DC bias supply voltage of 7.1 V via base bias resistors R17 and R16, and C7 rf decouples the base. Under normal conditions TR4 is biased off, because of the clamping voltage coupled to TR4 emitter by D6 and D7. However, under adverse conditions, ie if TR11 or TR12 are bottomed, either D6 or D7 conduct and TR4 is turned on. TR4 collector is connected to TR3 base via R10, therefore TR3 is turned on harder and the ALC1 controlling voltage increases, leading to a reduction in the rf signal fed to TR11 and TR12.

Transmitter Protection

18 Full transmit protection is provided on the PA unit, and is activated when the ALC1 voltage is outside normal limits. If, for whatever reason, the normal ALC feedback is unable to protect the PA, a signal is output on the Tx Protect, line J3/7, which (via the ATU) switches the equipment to Receive.

19 The ALC1 voltage is fed to the non-inverting input of IC1, via R3, with the inverting input referenced to +5 V via R5; C1 and C2 decouple both inputs. If the voltage on ALC1 rises above +5 V, the output of IC1 flips to the positive saturation limit of +5 V and puts a logic 1 on the Tx Protect line.

Tx/Rx SWITCHING (Fig 3.7.3)

20 The power amplifier only functions in the Tx mode, when the Tx/$\overline{\text{Rx1}}$ selection signal from Channelisation is at logic 1. This is inverted by IC2 and so TR13 is turned on. Once TR13 is switched on, +5 V is fed as a supply voltage to the driver stage and power output stage biasing circuits (TR14, TR15, TR16, TR17 etc.) and also to the thermal ALC circuit of TR18 and its associated components. TR7 also is switched on, by the double inversion of Tx/$\overline{\text{Rx1}}$, and this in turn switches on the constant current circuit of TR6, ZD3 and R18; it also switches on TR1 via base resistor R9 so that +15 V dc is supplied to the drain connection of the source follower TR2 in the ALC circuits.

21 In Rx mode, Tx/$\overline{\text{Rx1}}$ is logic 0 thus switching off TR13 and TR7 thereby removing the supply voltage from the biasing and ALC circuits. This conserves the Callpac battery.

+5 V and +15 V SUPPLIES (Fig 3.7.3)

22 In both Rx and Tx modes the +5 V dc is always present at J3/10 and is used as a voltage supply, by direct connection to IC1 and TR13 emitter and to TR15 and TR17. The +5 V dc supply is also used as a reference voltage for TR5, ZD4, and IC1 pin 2 (via R5).

23 The main supply line for the power amplifier is the +15 V switched supply, and this is fed into the PA on P1 via RLA1 on the Antenna Tuning Unit (ATU) when Tx mode is selected. The +15 V dc is fed to the primaries of T2 and T3 via rf chokes L2 and L7 and also to the ALC circuits via R6 and L1 with C3, C4, C18, C26 and C27 being rf decoupling capacitors. When the Callpac is in the Rx mode, RLA1 on the ATU is in the Rx position and +15 V is not supplied to the PA.

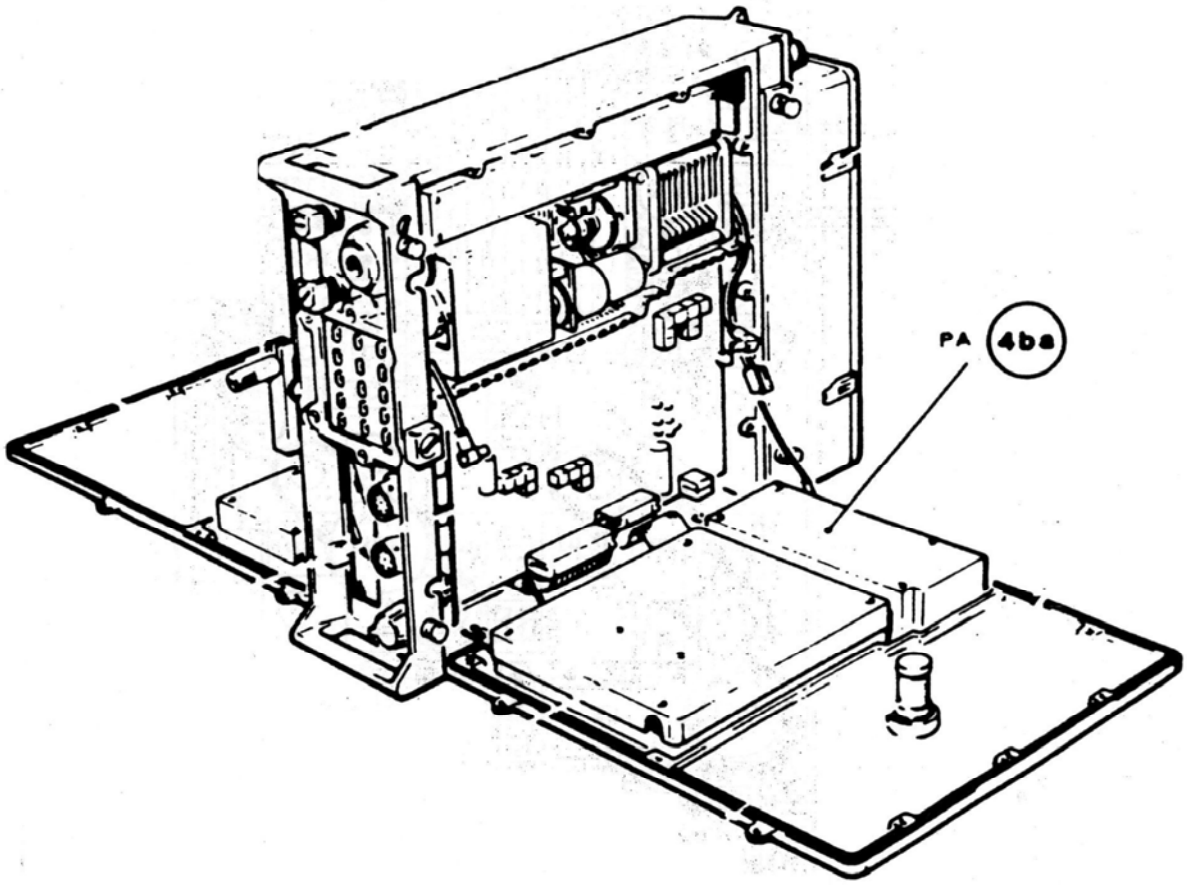

Fig 3.7.1 Power Amplifier PEC Location

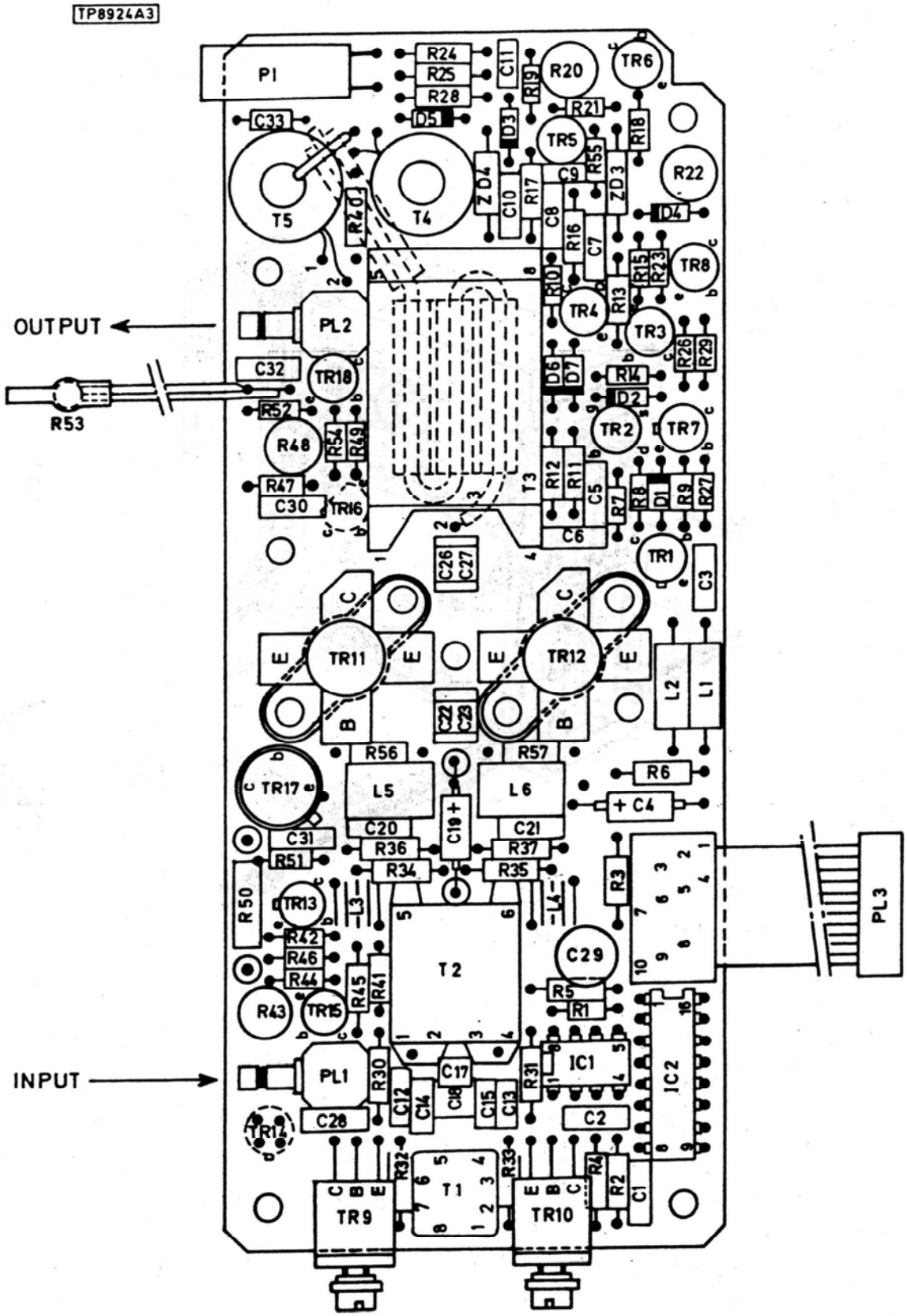

Fig 3.7.2 Power Amplifier PEC Component Location

TP10168A1

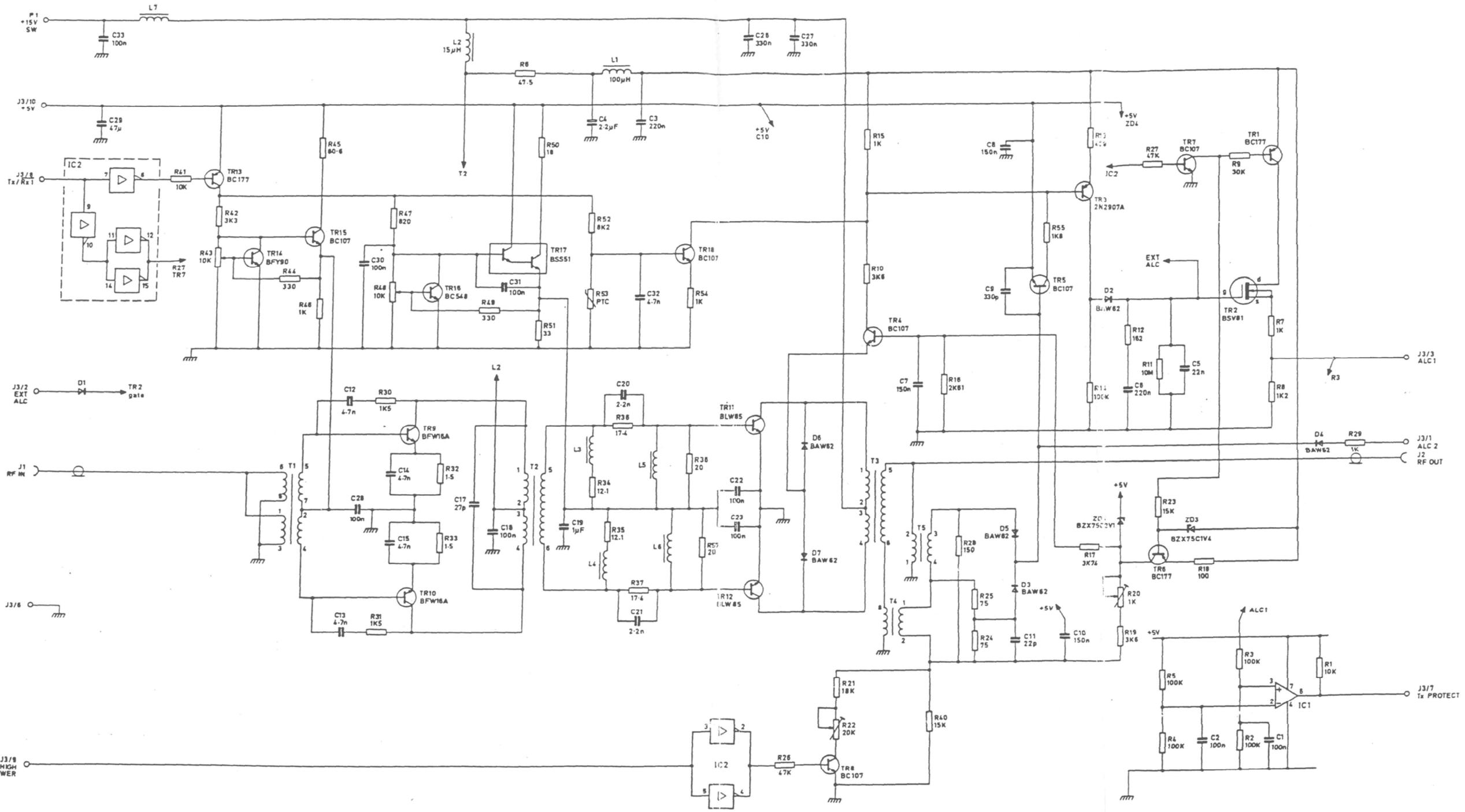

Fig 3.7.3 Power Amplifier Circuit Diagram Fig 3.7.3

CHAPTER 3.8

CASE CONNECTIONS

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CHAPTER 3.8

CASE CONNECTIONS

INTRODUCTION

1 This chapter describes those aspects of the Callpac radio that do not readily fall within the scope of previous chapters. All the elements described in this chapter are located either on the front panel or at the back of the Callpac radio. They are:

(a) Rotary Switch (S1A)

(b) Keyboard

(c) Liquid Crystal Display

(d) Audio Sockets (2) and AF Filtering PEC

(e) External supply and Battery Connections.

Fig 3.8.2 shows the interconnections between these elements and the other units of Callpac.

ROTARY SWITCH

2 S1A is a six-position switch that functions as an ON/OFF switch and also permits selection of five operational modes as follows:

(a) Handset control - H/S

(b) Keyboard control - K/B

(c) Store facility of pre-selected channels - STORE

(d) Keyboard control plus illumination of the display - K/B & ILL

(e) Full remote control - REM CON.

KEYBOARD

3 The front panel keyboard (S2), has twenty keys that enable an operator to perform the following functions:

(a) Cancel an entry or function

(b) Set the volume level

(c) Tune the antenna manually or automatically

(d) Select transmit power level

(e) Recall a stored channel

(f) Enter a new mode

(g) Enter a new frequency

(h) Increment the frequency

(j) Call a remote station or local operator

(k) Select Intercom operation

(l) Store a channel

(m) Examine the stored channels

(n) Erase the stored information.

Functions (a) to (k) are performed with the rotary switch set to K/B or K/B & ILL. To perform (l), (m) and (n) the rotary switch must be set to the STORE position.

4 The keyboard has 20 keys in a matrix of four rows and five columns. Each row and column is independently wired to the keyboard (1S2). The nine lines, four rows and five columns, are then connected to logic elements in Channelisation. The four row lines are normally held high (ie at logic 1) whilst the five column lines are held low (ie at logic 0). When the operator presses a key, one of the column lines is made high. The microprocessor contained in Channelisation is continuously scanning the logic levels present on the five column lines. Therefore it will detect that a high has been put onto one of the column lines. This initiates a routine (which is controlled by the microprocessor) that locates the actual key depressed. Once located the operation corresponding to key selection is controlled and/or performed by Channelisation.

LIQUID CRYSTAL DISPLAY

5 This provides visual data of operational parameters of the radio (eg mode, frequency, power setting etc). Its operation requires the following inputs:

(a) 12 data lines, DX 0 to DX 11

(b) 3 Strobe inputs, S0, S1 and S2

(c) Display light

(d) +5 V dc supply

(e) -6 V dc supply.

Note: The data lines for row and column keyboard information are interconnected on the display PEC but have no effect upon the operation of the display. (P1/1 to P1/9 and P2/1 to P2/9.)

6 The display PEC (Fig 3.8.1) contains the 8-digit 7-segment display (IC10), eight BCD-to-7-segment drivers (IC1 to IC8) and an astable multivibrator (IC9). BCD data is fed to the display PEC from Channelisation via the DX0 to DX11 input lines (P3/6 to P3/17). This data is connected directly to the eight drivers via the data input pins 2, 3, 4 and 5. The 7-segment outputs from the drivers (ie IC1 to IC8 pins a to g) are controlled by the display frequency input on pin 6. The display frequency input is provided by IC9 which is an astable multivibrator that produces a square wave output having a duty cycle of 50% at a frequency of 200 Hz approximately. When a square wave is present at the display frequency input of any of the drivers, the selected segments will have a square wave output that is 180° out of phase with the input. Those segments that are not selected will have a square wave output that is in phase with the input.

7 Data is transferred from input to output of the BCD drivers by the application of a high on the strobe inputs (C1 to IC8 pin 1). Three strobe inputs are fed from Channelisation; S0 is connected to P3/18 on the display PEC and latches IC1 and IC2. S1 is connected to P3/19 and latches IC3, IC4 and IC5. S2 is fed to P3/20 and latches IC6, IC7 and IC8. The display frequency for input to the drivers is fed from IC9 pin 10 output via R5. The other output at IC9 pin 11 is in antiphase to the plane display frequency and is connected to the display. The back of the display is connected to IC9 pin 10 via dc blocking capacitor C4. Each of the eight digits of the display is driven by one BCD-to-7 segment driver. Any segment that has a voltage across it will appear black on a white background. Therefore when the square wave signal on any of the segment input lines, IC10, A1, B1, C1, D1, E1, G1, F1 etc, is in anti-phase to the square wave signal on the back plane of the display that segment will appear black. (See Fig 3.8.3).

8 The decimal points on the display are not variable and therefore remain lit all the time. The display can be illuminated for low ambient light conditions by two lamps mounted on the display PEC (DS1 and DS2). These are connected to +5 V by limiting resistors R7 and R8. The two lamps are coupled to Channelisation via P3/4. A transistor switching circuit mounted in Channelisation switches the lamps on and off (see Table 3.8.1).

AUDIO SOCKETS AND FILTERS

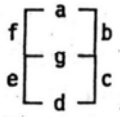
9 There are two audio sockets on the front panel. Each audio socket has seven pins which are wired to the AF filtering PEC (1a). The PEC is shown on the Case and Sub-unit Assembly Circuit (Fig 3.8.2).

Audio Socket One, SK1

10 Pin A of SK1 is the MIC 1 audio input. This is fed to PL2-2 of Phasing via a low pass balanced pi filter, L8, L9, C13 and C14. The common rail for the microphone input is connected to SK1-B. The Battery Switched supply of +15 V is available at SK1-C with filtering and limiting provided by R1, L11, C16 and C17. This voltage is fed from the rotary switch (S1A), via TB1-1 of the AF filtering PEC. Interconnection is also made at this point to connect this supply to Phasing (1a, PL1 pin 8 to 1d, PL2 pin 8). Audio output from Phasing is fed to SK1-D via 1d, PL2 pin 10 and 1a, PL1 pin 10. Audio SK1-E is connected to the 0 V line. The pressel for audio socket 1 is coupled to SK1-F, and when the pressel is depressed this pin goes to 0 V. This results in a pressel command signal of logic '0' being put on the pressel line to Channelisation, which then produces controlling logic that enables the audio inputs to Phasing.

Table 3.8.1 BCD Code to Character Conversion

INPUT CODE						OUTPUT STATE							DISPLAY CHARACTER
IC1 to IC8 PIN NUMBER						IC1 to IC8 PIN NUMBERS							
4	2	3	5			9	10	11	12	13	15	14	
2^3	2^2	2^1	2^0			a	b	c	d	e	f	g	
0	0	0	0			1	1	1	1	1	1	0	0
0	0	0	1			0	1	1	0	0	0	0	1
0	0	1	0			1	1	0	1	1	0	1	2
0	0	1	1			1	1	1	1	0	0	1	3
0	1	0	0			0	1	1	0	0	1	1	4
0	1	0	1			1	0	1	1	0	1	1	5
0	1	1	0			1	0	1	1	1	1	1	6
0	1	1	1			1	1	1	0	0	0	0	7
1	0	0	0			1	1	1	1	1	1	1	8
1	0	0	1			1	1	1	1	0	1	1	9
1	0	1	0			0	0	0	1	1	1	0	L
1	0	1	1			0	1	1	0	1	1	1	H
1	1	0	0			1	1	0	0	1	1	1	P
1	1	0	1			1	1	1	0	1	1	1	A
1	1	1	0			0	0	0	0	0	0	1	-
1	1	1	1			0	0	0	0	0	0	0	



DISPLAY CHARACTER

11 SK1-G is the standby signal line, which is connected to Channelisation 1c, PL2 pin 10 via a pi filter and TB1 pin 2 of the filtering PEC. The Standby line is only functional when the Special Handset is being used. When the Special Handset is fitted, the standby line (SK1-G) is connected to SK1-E in the off position of the handset volume adjust. This puts a logic '0' on the Standby line, which effectively switches off the Callpac power supply unit, thereby conserving battery power.

Audio Socket Two, SK2

12 Pin A of SK2 is the MIC 2 audio input. This is fed to PL2-1 of Phasing via a low pass balanced pi filter network. The common rail for the microphone input is connected to SK2-B. For full remote operation, auxiliary remote equipment has to be connected to the Audio 2 socket (SK2). SK2-C is the enabling remote control input, which is fed to Channelisation via interconnections in Phasing. Connection from SK2-C to Phasing is made via a low pass pi filter and 1a, PL1 pin 4. Audio output to audio SK2 is connected to pin D. SK2-E is an earth terminal, whilst the pressel line is connected to SK2-F.

13 If a morse key is to be used with the Callpac instead of audio equipment it must be connected to the Audio 2 socket (SK2). The key input for morse operation is fed to

Channelisation via SK2-G and interconnections in Phasing. A summary of Audio Socket and AF filtering PEC connections is given in Table 3.8.2.

Table 3.8.2 Summary of Audio Socket and AF Filtering PEC Connections

SK1 PIN No	TITLE	1a PIN No	CONNECTED TO	REMARKS
A	MIC 1	PL1-2	1d, PL2-2	Audio I/P
B	0 V MIC	PL1-3	1d, PL2-3	Audio Common
C	Batt SW	TB-1 PL1-8	S1A-2 1d, PL2-8	Batt positive Switched Supply
D	AF O/P	PL1-10	1d, PL2-10	SK1 D connected to SK2 D
E		PL1-9	Earth	
F	Pressel 1	PL1-6	1d, PL2-6	Then fed to Channelisation
G	Standby	TB1-2	1c, PL2-10	Only used with Special H/S
A	MIC 2	PL1-1	1d, PL2-1	Audio I/P
B	0 V MIC	PL1-3	1d, PL2-3	Audio Common
C	FR/PLUG	PL1-4	1d, PL2-4	Only used with Remote
D	AF O/P	PL1-10	1d, PL2-10	Also connected to SK1-D
E		PL1-9	Earth	
F	Pressel 2	PL1-5	1d, PL2-5	Then fed to Channelisation
G	Key	PL1-7	1d, PL2-7	Then fed to Channelisation

EXTERNAL SUPPLY AND BATTERY CONNECTIONS (Fig 3.8.2)

Battery Connection

14 The Callpac battery fits into a compartment located at the back of the radio. When fitted, the positive (+) and negative (-) terminals of the battery connect to PL5 pins 2 and 1 respectively.

External Supply

15 The external supply is connected to the Callpac via PL1, which is located on the back case of the radio. The positive supply line is fed in on PL1 pin A, whilst the negative connection is made to pin B.

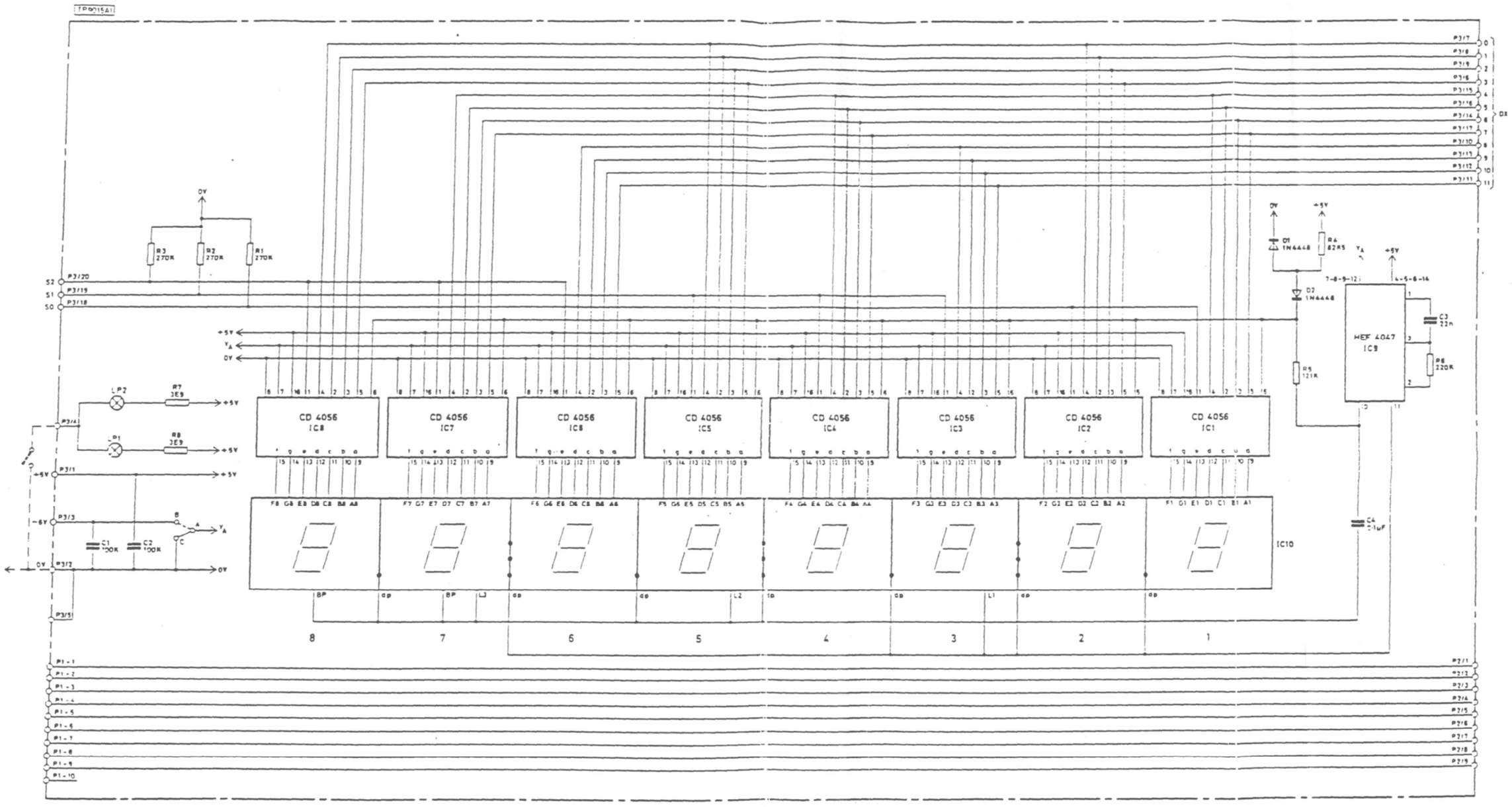
Battery Charging

16 The Callpac battery is a rechargeable Nicad battery having an operational capacity of approximately 10 hours continuous transmit or up to 120 hours under receive-only conditions. There are several types of battery charger that can be used with the Callpac, eg hand-crank generator, solar cells etc (see Part 4 of Callpac Accessories Manual PN1599), but all of these supply a charging current via PL1 pin D. This pin is connected to 1b pin 3. When charging the battery a charging current flows to the battery via PL1 pin D, 1b pin 3, 1b pin 5 and PL5 pin 3. The diode, D3, mounted on the protection PEC is fitted in series with the charging current path as an isolator.

17 The Callpac can be fitted with an optional internal battery charger. If fitted, this charger is located in Channelisation and is supplied with a positive dc supply via PL1 pin D. The charging current supplied by the internal battery charger flows from Channelisation to the battery via interconnecting links on the power supply unit and the protection PEC.

VHF/HF System Consideration

18 The Callpac radio can be used with the 4600 VHF station in a combined VHF/HF System. When used in this way both the Callpac and the 4600 radios may be supplied from a single source ac external power supply. This power supply is incapable of providing a supply to both radios if they are both operating in high power modes. Therefore one or both of them must be kept in the low power mode. External low power selection of the Callpac radio is enabled when a low is put on to PL1 pin C, which is connected to the external ac power supply when operating the Callpac in a combined VHF/HF System. PL1 pin C is connected to J1/10 in Channelisation via interconnecting links on the power supply unit. When a low is put on PL1 pin C the Callpac can only transmit in the low power mode.



Display PEC Circuit Diagram

Fig 3.8.1

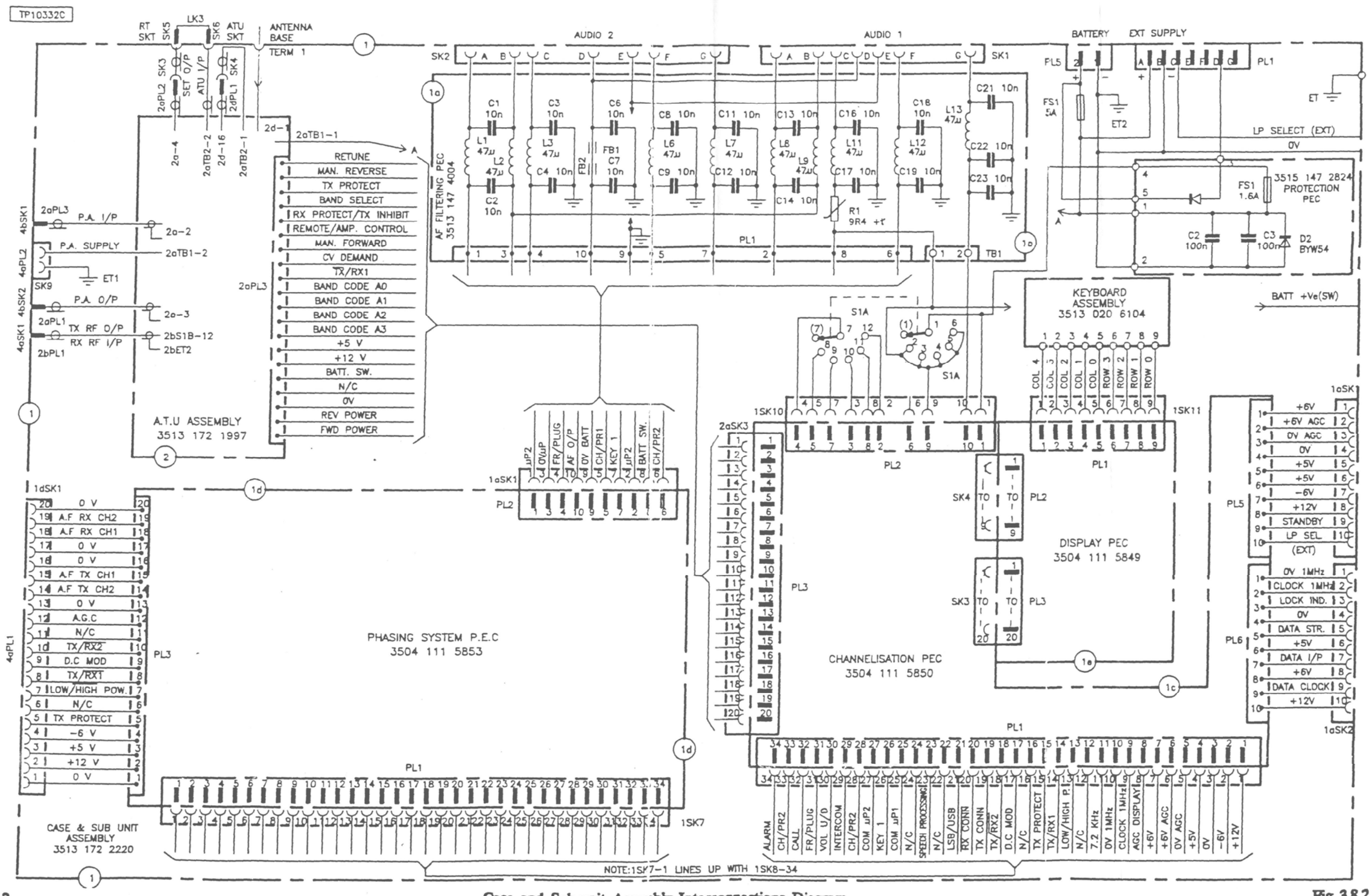


Fig 3.8.2 **Case and Sub-unit Assembly Interconnections Diagram** Fig 3.8.2

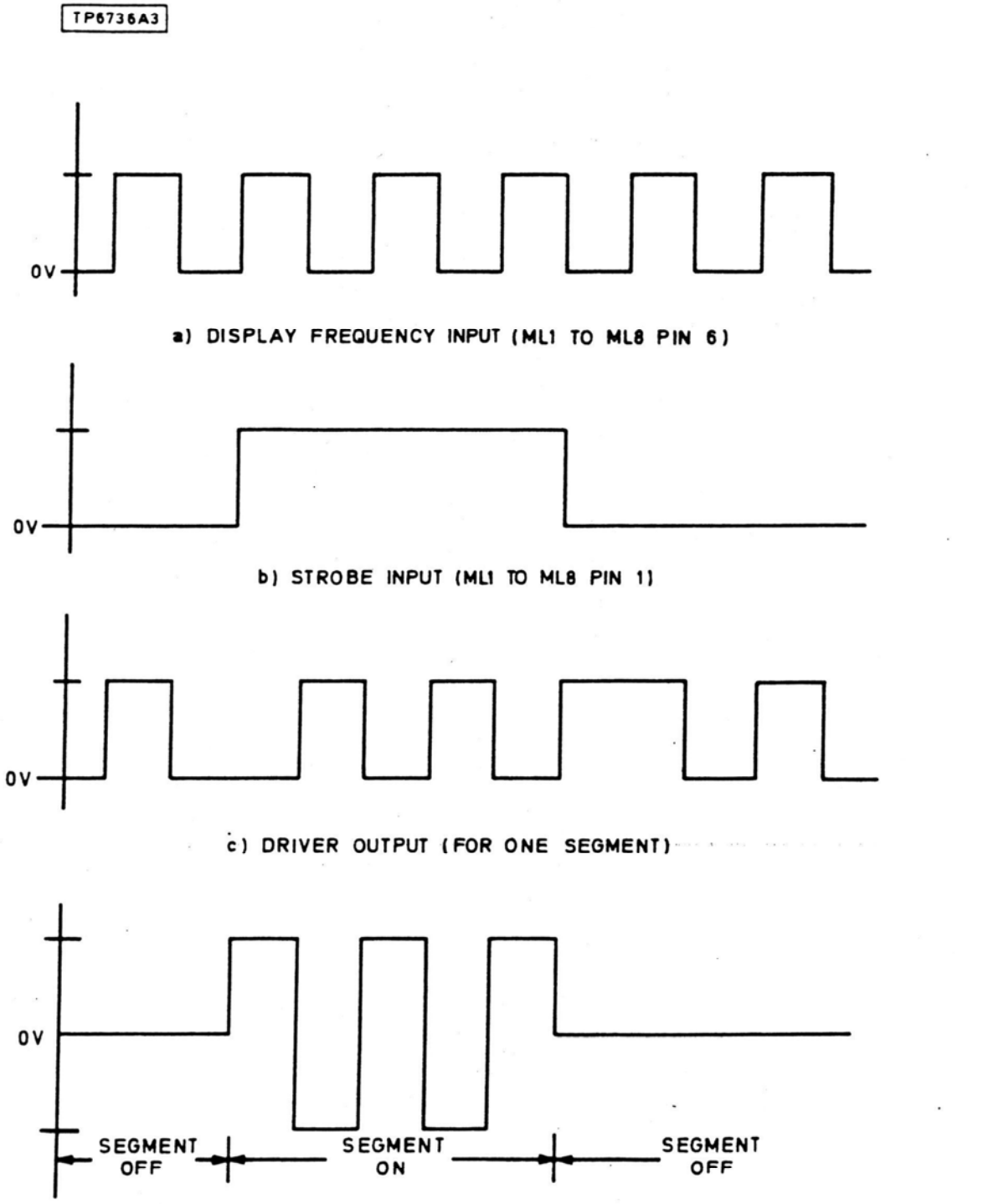


Fig 3.8.3 Liquid Crystal Driver Waveforms

CHAPTER 5.1

2nd LINE MAINTENANCE INFORMATION AND INSTRUCTIONS

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CHAPTER 5.1

2nd LINE MAINTENANCE INFORMATION AND INSTRUCTIONS

INTRODUCTION

1 The information contained in this Category is intended to support second-line fault diagnosis and repair. Second-line servicing consists of repair-by-replacement of modules identified as malfunctioning or suspect during testing. No subsequent adjustment or alignment is required.

2 Transceivers accepted for repair must first be tested in accordance with the first-line functional test procedure, detailed in Category 2, to confirm that a fault exists. Once a fault has been confirmed the procedures commencing at para 17 must be followed in order to isolate the fault to a particular module. Module removal and replacement procedures are given in para 35 to 53.

3 Before the transceiver is returned to the operator it must be tested for leakage from the seals. Carry out the procedure given at para 54. On successful conclusion of the test replace the desiccant using the procedure given at para 38.

SPECIAL TOOLS, ACCESSORIES AND TEST EQUIPMENT

Special Tools

4 4.1 Desiccant Extractor Tool, MCT 30795

4.2 Ribbon Connector Extractor

4.3 Pressurising Adaptor, MC 50106

Special Accessories

5 Memory Store Key, BA 1233

Test Equipment

6 Items of test equipment for second-line servicing are listed in Table 5.1.1.

TEST SET TS 2010

Introduction (Fig 5.1.1)

7 Tests detailed within this Category are based on the use of the Test Set TS 2010. Where necessary, additional test equipment is called for, and this is detailed in the Test Routine Tables.

8 The test set is housed in a rectangular box which also houses the cables and probes supplied with it. The test set lid is fitted with a chart, identifying the tests by letter and the cables to be used for each test.

9 The following functions are performed by the test set:

(a) Direct current and voltage measurements, and continuity checking

(b) High-frequency signal voltage measurements

(c) Sensitivity measurements

(d) Transceiver dynamic range measurements

(e) Transmitter output power measurements

10 Measurement results are displayed on a row of 15 light emitting diodes (LED). Two further LED are used as internal battery charging (INT BATT CHARGE) and test set power (ON) status indicators.

Table 5.1.1 Test Equipment

Type/Ref No	Nomenclature	No Off	Remarks
BA 1268	Test Set TS 2010 containing:	1	
CX 2010	Cable	1	RF Measurement
CX 2011	Cable	1	Transceiver Current Measurement
CX 2012	Cable	1	DC Measurement/Current
CX 2013	Cable	1	DC Measurement/Battery Charging
	Probes (Red/Black)	Set	
CX 2014	Cable	1	AF Measurement/Transceiver Battery
CX 2015	Cable	1	HF Measurement (mv)
9571 113 4500	Test Accessories comprising:	Set	
3513 171 3336	Coax cable (female/male)	2	
3513 171 3337	Coax cable (male/male)	1	
3513 171 3338	PA Supply Extension Lead	1	
BA 1338	PSU Interface Test Unit	1	
BA 1339	Synthesiser Test Unit	1	
BA 1340	Channelisation/Phasing Test Connector	1	
BA 1341	ATU/Phasing Test Connector	1	
BA 1342	AF Adaptor and Test Plugs	1	
BA 1343	Dummy Antenna	1	

Battery Charging

11 Flashing or non-illumination of the ON LED, when the ON pushbutton is operated, indicates that the test set internal battery requires recharging.

CAUTION: TO AVOID DAMAGE TO THE BATTERY DO NOT RECHARGE UNLESS INDICATED.

12 To charge the battery the following procedure should be adopted.

(1) Connect cable CX 2013 to the CALLPAC socket on the test set.

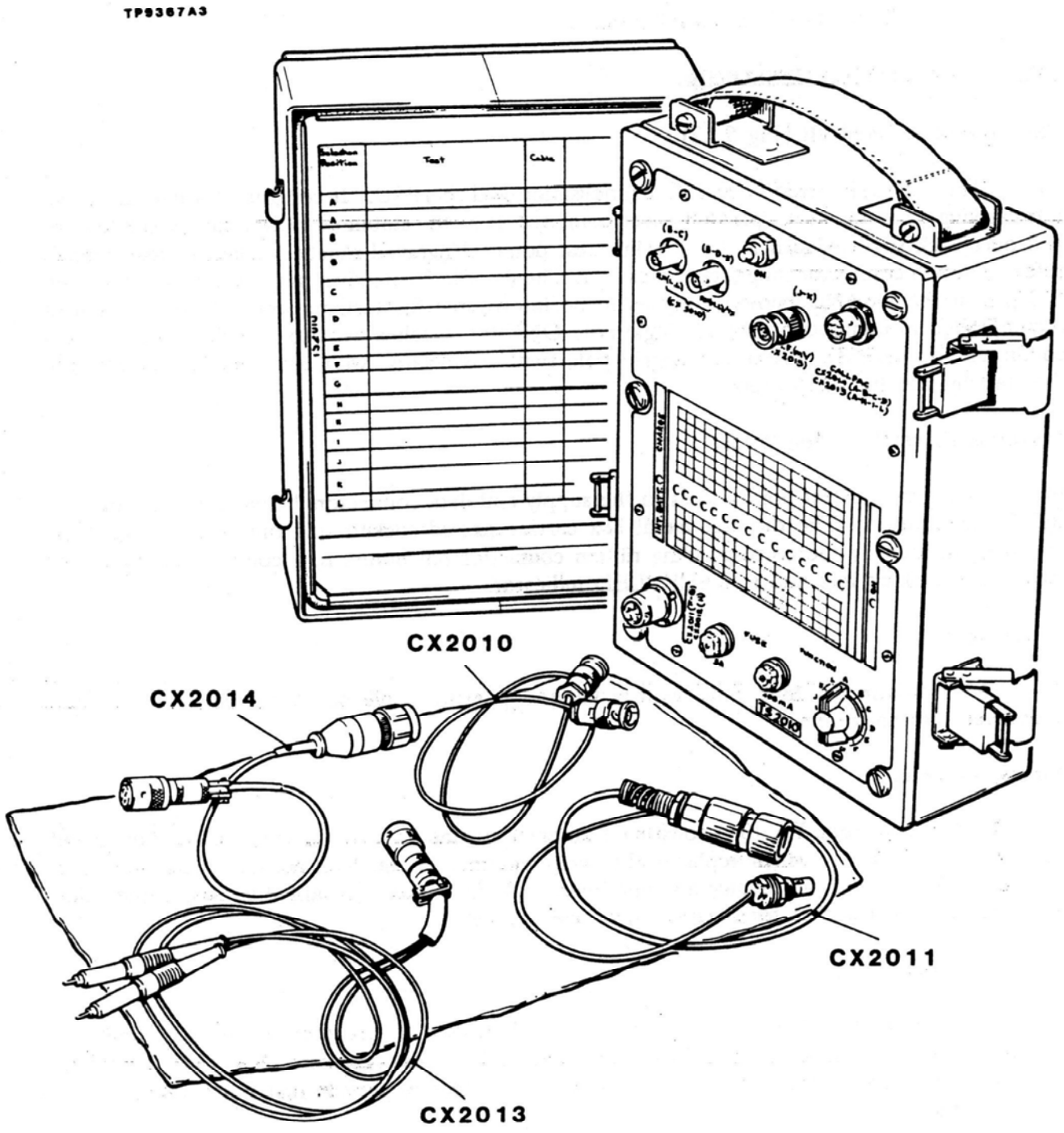


Fig 5.1.1 Test Set TS 2010

(2) Set the test set FUNCTION switch to Position H.

(3) Connect the free ends of Cable CX 2013 to a 12 V to 32 V dc supply. Red to positive, black to negative. The INT BATT CHARGE LED should illuminate.

(4) Allow 14 hours for full charge.

TEST UNITS AND ACCESSORIES

PSU Interface Test Unit (Fig 5.1.2)

13 This unit is inserted between Channelisation and the PSU. It consists of a die cast metal box carrying 12 red sockets, providing test point access to the stabilised power supply connectors, and one black socket which is the 0 V line test point. Engraved numbers adjacent to terminals refer to ribbon connector plug/socket pins. Five single pole changeover switches marked O/C and S/C permit the individual power supplies to be interrupted for test purposes. The switching is accomplished in conjunction with 5 single pole ON/OFF switches used to introduce dummy load conditions for the PSU. A further single pole switch associated with pin 9 enables earthing of the standby line for test purposes.

Synthesiser Test Unit (Fig 5.1.2)

14 This provides test point access to the supply and data connectors between the Synthesiser and Channelisation. The die cast metal box carries six red sockets and one black socket with engraving to identify the corresponding ribbon connector pin numbers, a coaxial connection for access to the clock line and a 'LOCK' LED indicator.

AF Adaptor

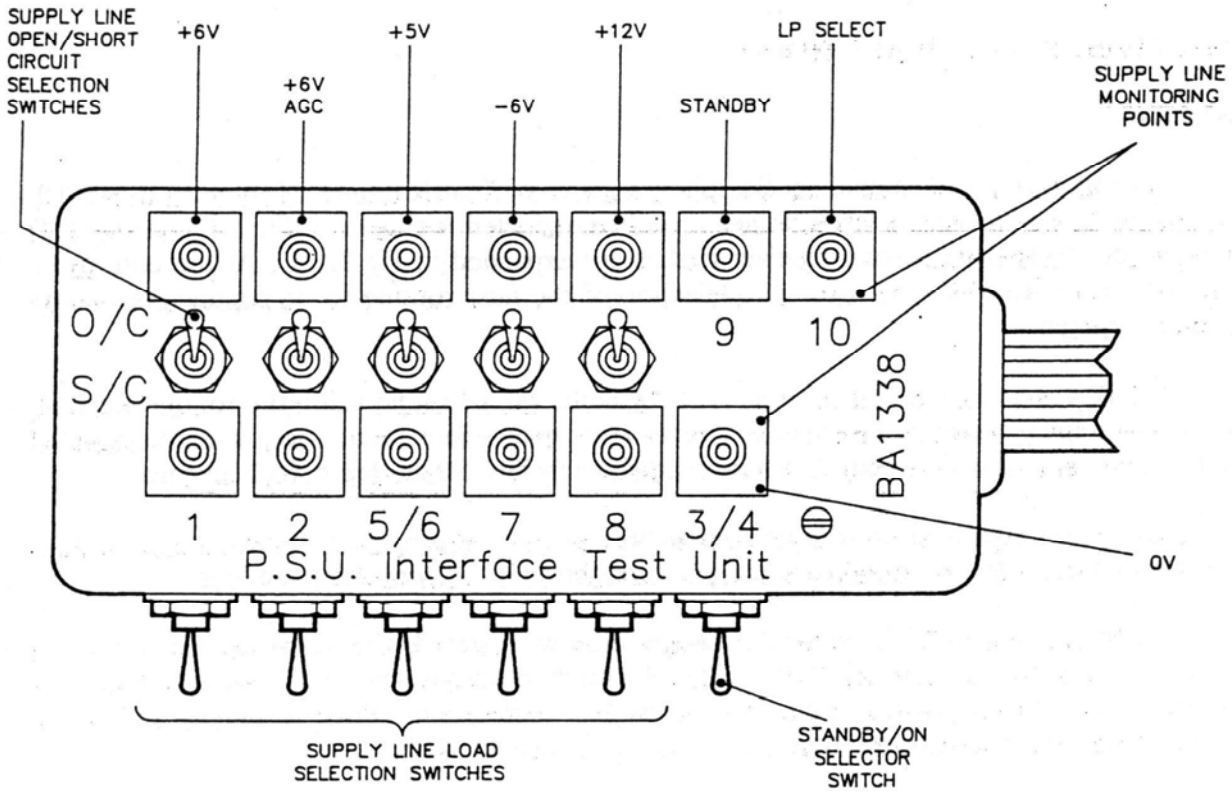
15 AF Adaptor BA 1342 mates with a handset plug to enable an audio check to be made at selected internal points.

Dummy Antenna

16 Dummy Antenna BA 1343 consists of an encapsulated load, comprising a series-connected inductor and capacitor, which replaces the whip antenna in the Transmitter Check and Test Routines. One end of the dummy antenna mates with the transceiver antenna socket, the other terminates in a test socket for connection to the test set.

Test Connectors

17 Test connector BA 1341 fulfils a dual role. It is used to interconnect the RF Head and Phasing or to interconnect Channelisation and the ATU. Test connector BA 1340 is used to interconnect Channelisation and Phasing. Both test connectors provide test point access to the interconnected lines.



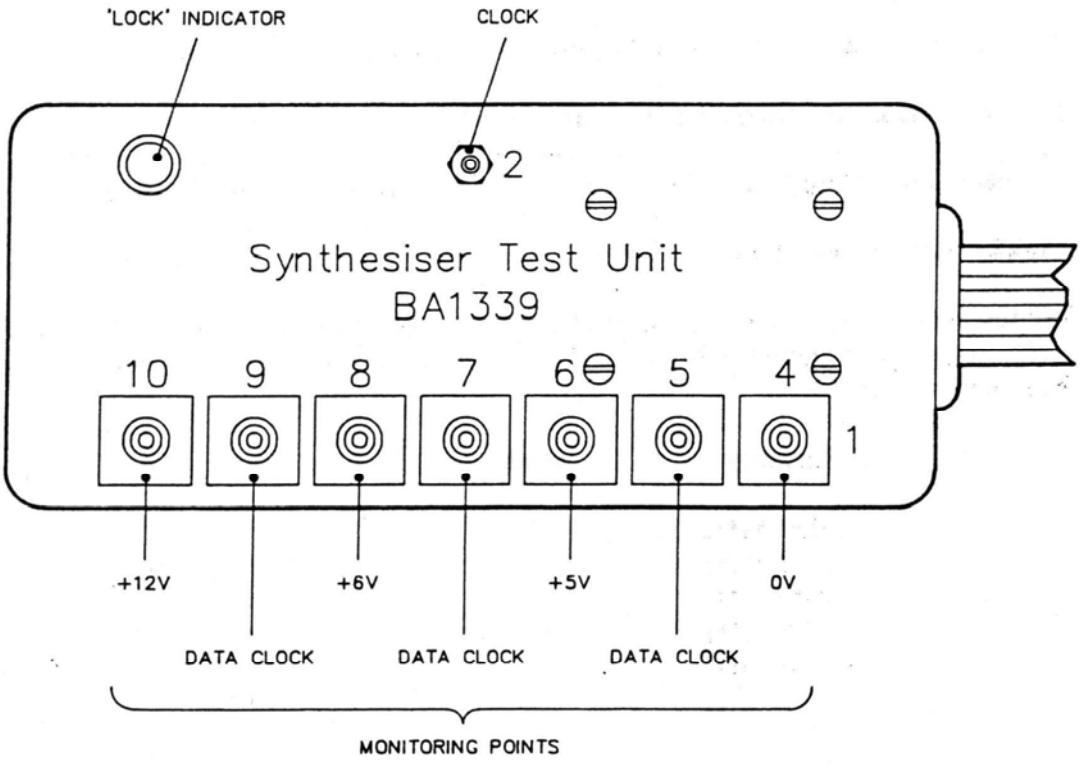


Fig 5.1.2 Test Units

TRANSCEIVER FUNCTIONAL CHECKS

Introduction

18 The transceiver functional checks follow a series of Test Routines (Tables 5.1.2 to 5.1.10). The sequence in which these test routines must be conducted is shown in Fig 5.1.3, and the Test Routines for the transmitter and receiver checks are expanded in Fig 5.1.4. At the conclusionof each routine, return to Fig 5.1.3 for an indication of the next routine to be conducted, or action to be undertaken.

19 While it is anticipated that the majority of faults will be found using the routines as stated, if an obscure fault causes a return to the same start point more than twice, it is recommended that the equipment be returned to a base workshop facility for in-depth fault diagnosis.

20 The power supply test routine provides three possible action options. If the apparent fault is not cleared after the first optional action, work through the remaining options.

21 When conducting Test Routines, unless otherwise stated, the transceiver rotary switch must be set to K/B, the test set FUNCTION switch must be set to the corresponding test position, and the test connectors and cables must also correspond. Prior to making or breaking any connections, the transceiver rotary switch must be set to OFF.

CAUTION: TO AVOID DAMAGE, RIBBON CONNECTORS MUST BE DISCONNECTED USING THE EXTRACTOR TOOL.

Initial Setting-up

22 Before commencing test routines the following procedures must be conducted:

(1) Ensure transceiver rotary switch is set to OFF.

(2) Connect power supply unit, adjusted to 15 ±1 V, to the external connector.

(3) Check serviceability of fuse (5 A).

(4) If the serviceability of the equipment permits, set transceiver rotary switch to K/B and, using the Memory Store Key BA 1233, store the following data in the channels indicated:

Channel	Frequency	Mode
0	5.0000 MHz	3
1	1.8750 MHz	3
2	2.5000 MHz	3
3	3.7500 MHz	3
4	5.6250 MHz	3
5	9.3750 MHz	3

Channel	Frequency	Mode
6	13.1250 MHz	3
7	16.2500 MHz	3
8	25.6250 MHz	3
9	29.3750 MHz	3

If this is not possible, any frequency required must be entered manually into working channel.

(5) Connect handset to AUDIO 2.

(6) Refer to Fig 5.1.3.

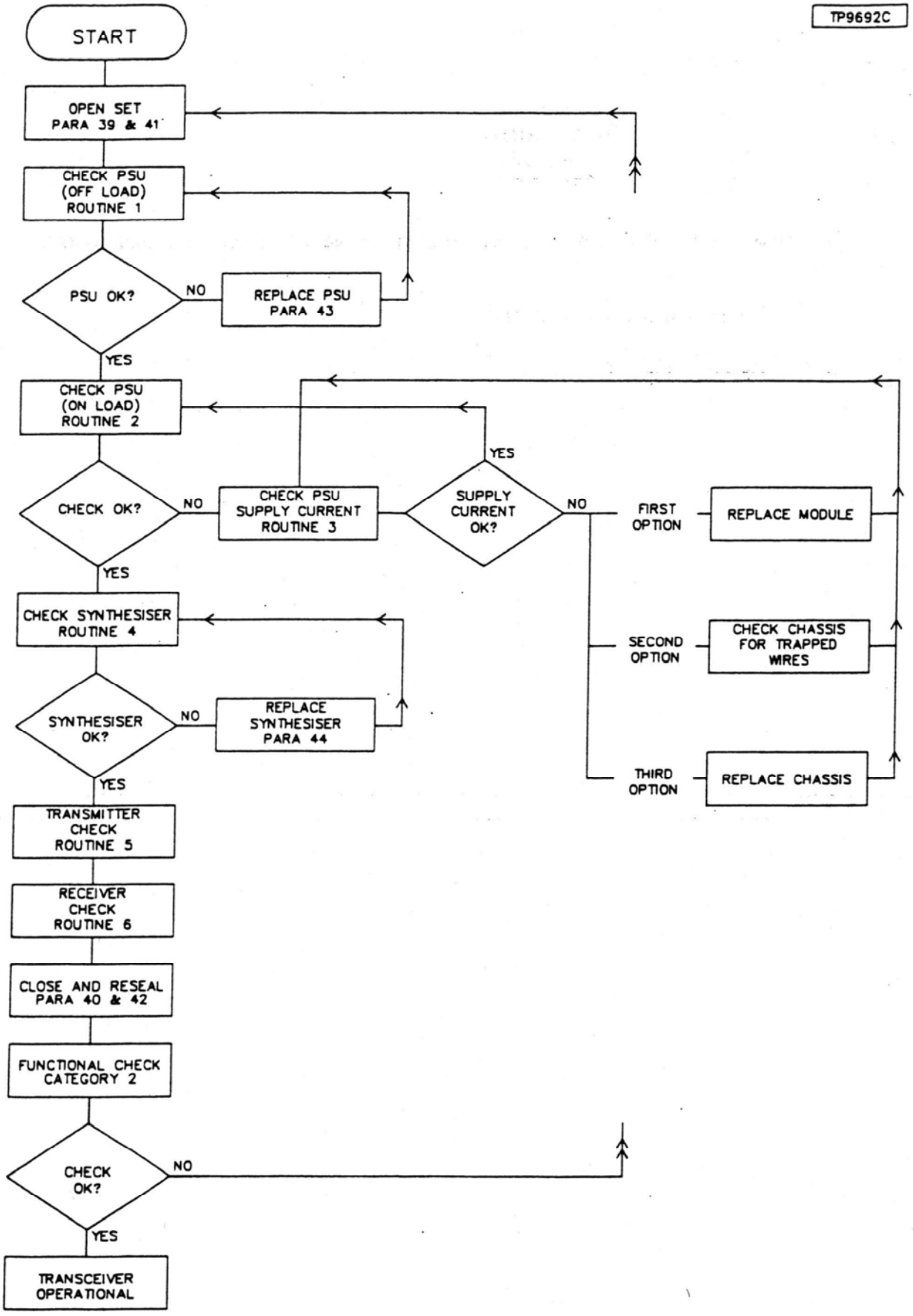


Fig 5.1.3 Overall Functional Check - Flow Diagram

Test Routine 1 - Check PSU (Off-load)

23 Refer to Table 5.1.2 and Fig 5.1.2, 5.1.3 and 5.1.7.

Table 5.1.2 Test Routine 1 - Check PSU (Off-load)

Step	Action	Indication
1	Remove PSU Lid (Fig 5.1.7 item J) and connect PSU Interface Test Unit BA 1338 as shown in Fig 5.1.7 between Channelisation and PSU plug.	
2	On test unit (Fig 5.1.2) set the five OC/SC switches to OC.	
3	On test unit, set the five load switches and the Standby/On selector switch to ON.	
4	Connect cable CX 2013 between the test set and the test unit, black lead to PL1-3/4 (0 V) and the red lead as directed at Step 8.	
5	Set test set FUNCTION switch to position A.	
6	Set transceiver rotary switch to K/B.	
7	On test set, press and hold ON switch and monitor the LED indication while conducting Step 8.	
8	Connect the red lead of cable CX 2013 to each of the following points in turn:	
	PSU-1 (+6 V)	5
	PSU-2 (6 V AGC)	5
	PSU-5/6 (+5 V)	4
	PSU-8 (+12 V)	11
	PSU-9 (14.5 V standby)	12 or 13
	PSU-10 (LP select)	0
9	Release ON switch.	
10	Set transceiver rotary switch to OFF.	
11	On test unit, transfer cable CX 2013 black lead to PSU-7 (-6 V) and red lead to PSU-3/4 (0 V).	
12	Set transceiver rotary switch to K/B.	
13	On test set, press and hold ON switch and monitor LED indication.	5
14	Release ON switch.	
15	Set transceiver rotary switch to OFF.	
16	Refer to Fig 5.1.3	

Test Routine 2 - Check PSU (On-load)

24 Refer to Table 5.1.3, and Fig 5.1.2 and 5.1.3.

Table 5.1.3 Test Routine 2 - Check PSU (On-load)

Step	Action	Indication
1	On test unit, set load switches, except Standby/ON switch associated with PSU-9, to OFF.	
2	On test unit, set the five OC/SC switches to SC.	
3	Connect cable CX 2013 black lead to PL1-3/4 (0 V) and the red lead as directed at Step 7.	
4	Connect dummy load.	
5	Set transceiver rotary switch to K/B.	
6	Tune transceiver to 5.6250 MHz, Mode 3.	
7	On test set, press and hold ON switch and monitor LED indication while conducting Step 7.	
8	Connect the red lead of cable CX 2013 to each of the following points in turn:	
	PSU-1 (+6 V)	5
	PSU-2 (6 V AGC)	5
	PSU-5/6 (+5 V)	4
	PSU-8 (+12 V)	11
	Operate the handset pressel and hold	
	PSU-8 (+12 V)	11
	Release the handset pressel	
	PSU-9 (Standby 14.5 V)	13 or 14
	PSU-10 (LP select)	2 or 3
9	Release ON switch.	
10	On test unit, transfer cable CX 2013 black lead to PSU-7 (-6 V) and red lead to PSU-3/4 (0 V).	
11	On test set, press and hold ON switch and monitor LED indication	5
12	Operate handset pressel and monitor LED indication.	5
13	Release ON switch.	
14	Set transceiver rotary switch to OFF.	
15	Remove cable CX 2013 from test set to test unit.	
16	Refer to Fig 5.1.3	

Test Routine 3 - Check PSU Supply Current

25 Refer to Table 5.1.4, Fig 5.1.2, 5.1.3 and 5.1.7.

Table 5.1.4 Test Routine 3 - Check PSU Supply Current

Step	Action	Indication
1	Unplug the following ribbon connectors: (a) Synthesiser to Channelisation (b) Channelisation to Phasing (c) Channelisation to ATU (d) Phasing to RF Head	
2	Connect cable CX 2012 to the test set. **Note:** Black and red leads are connected, in turn, across red terminals above and below the five OC/SC switches on the test unit (black lead to top terminal). Measurements are taken by setting the appropriate OC/SC switch to OC. After each measurement, return the OC/SC switch to SC. If, at the end of a particular test, any indication is incorrect, refer to the options shown on Fig 5.1.3 and take appropriate action with the unit most recently connected.	
3	Connect dummy load and ensure link fitted.	
4	At the test unit, ensure all OC/SC switches are set to SC.	
5	Set test set FUNCTION switch to position H.	
6	Set transceiver rotary switch to K/B.	
7	On test set, press and hold ON switch and monitor LED indication while conducting Step 8.	
8	Connect cable CX 2012 red and black leads to each of the following points in turn: PSU-8 (+12 V) PSU-5/6 (+5 V) PSU-1 (+6 V) PSU-2 (6 V AGC) PSU-7 (-6 V) (reverse connection)	0 15 (see Note:) 0 0 0
9	Release ON switch.	
10	Set transceiver rotary switch to OFF.	
11	Reconnect ribbon connector removed in Step 1(a).	

Note: Indication will be 0 if new channelisation PEC fitted - 3504 114 27840.

Table 5.1.4 Test Routine 3 - Check PSU Supply Current (Contd)

Step	Action	Indication
12	Repeat Steps 6 to 10 to measure current taken from each of the supplies with the Synthesiser connected.	
	PSU-8 (+12 V)	7 to 9
	PSU-5/6 (+5 V)	2 or 3
	PSU-1 (+6 V)	0
	PSU-2 (6 V AGC)	0
	PSU-7 (-6 V) (reverse connection)	0
13	Reconnect ribbon connector removed in Step 1(b).	
14	Repeat Steps 6 to 10 to measure current taken from each of the supplies with the Synthesiser and Phasing connected.	
	PSU-8 (+12 V)	8 or 9
	PSU-5/6 (+5 V)	3 or 4
	PSU-1 (+6 V)	0
	PSU-2 (6 V AGC)	0
	PSU-7 (-6 V) (reverse connection)	0
15	Reconnect ribbon connector removed in Step 1(c).	
16	Repeat Steps 6 to 10 to measure current taken from each of the supplies with the Synthesiser, Phasing and ATU connected.	
	PSU-8 (+12 V)	8 to 10
	PSU-5/6 (+5 V)	3 or 4
	PSU-1 (+6 V)	0
	PSU-2 (6 V AGC)	0
	PSU-7 (-6 V) (reverse connection)	0
17	Reconnect ribbon connector removed in Step 1(d).	
18	Repeat Steps 6 to 10 to measure current taken from each of the supplies with the Synthesiser, Phasing PEC, ATU and RF Head PEC connected.	
	PSU-8 (+12 V)	10 to 12
	PSU-5/6 (+5 V)	15
	PSU-1 (+6 V)	0
	PSU-2 (6 V AGC)	0
	PSU-7 (-6 V) (reverse connection)	0 or 1
19	Set transceiver rotary switch to K/B.	
20	At the transceiver, select Low power (4 watt).	

Table 5.1.4 Test Routine 3 - Check PSU Supply Current (Contd)

Step	Action	Indication
21	Operate the transmit pressel and hold while conducting Step 22.	
22	Repeat Steps 7 to 10 to measure current taken in transmit mode.	
	PSU-8 (+12 V)	15
	PSU-5/6 (+5 V)	15
	PSU-1 (+6 V)	0
	PSU-2 (6 V AGC)	0
	PSU-7 (-6 V) (reverse connection)	1 or 2
23	Disconnect PSU Interface Test Unit BA 1338 and remake cable connections.	
24	Replace PSU lid and secure in position.	
25	Refer to Fig 5.1.3	

Test Routine 4 - Check Synthesiser

26 Refer to Table 5.1.5, and Fig 5.1.2, 5.1.3 and 5.1.8.

Table 5.1.5 Test Routine 4 - Check Synthesiser

Step	Action	Indication
1	Connect Synthesiser Test Unit BA 1339 as shown in Fig 5.1.8 between Channelisation and Synthesiser plug. **Note:** If the LED indications are incorrect for any of the following tests, replace the Synthesiser and repeat tests.	
	Supply and Data Input Test	
2	Connect cable CX 2013 between the test set and the test unit, black lead to PL1-1/4 (0 V) and the red lead as directed at Step 7.	
3	Set test set FUNCTION switch to position A.	
4	Set transceiver rotary switch to K/B.	
5	Tune transceiver to 5.0000 MHz, Mode 3.	
6	On test set, press and hold ON switch and monitor LED indication while conducting Step 7.	
7	Connect the red lead of cable CX 2013 to each of the following points in turn:	
	PL1-10 (+12 V)	10 to 12
	PL1-8 (+6 V)	4 to 6
	PL1-6 (+5 V)	3 to 5
	PL1-5 (Data Strobe)	1
	PL1-9 (Data Clock)	1
	PL1-7 (24 bit data stream:	
	Even 100 Hz Steps	1
	Odd 100 Hz Steps)	9 or 10
8	Set transceiver rotary switch to OFF.	
9	Disconnect Cable CX 2013.	
	Clock Test	
10	Set test set FUNCTION switch to position J.	
11	Set transceiver rotary switch to K/B.	

Table 5.1.5 Test Routine 4 - Check Synthesiser (Contd)

Step	Action	Indication
12	Check that transceiver is still tuned to 5 MHz, Mode 3.	
13	Connect coax cable CX 2015 between the test set and the test unit.	
14	On test set, press and hold ON switch and monitor LED indication.	3 to 5
15	Set transceiver rotary switch to OFF.	
16	Disconnect cable CX 2015 from test unit.	
	VCO Output Test	
17	Disconnect coax cable from Synthesiser to RF Head.	
18	Connect the miniature coax end of cable CX 2015 to the coax cable disconnected at Step 17, using miniature coax cable (Male/Male) 3513 171 3337.	
19	Set test set FUNCTION switch to position J.	
20	Set transceiver rotary switch to K/B.	
21	On test set, press and hold ON switch and monitor LED indication while conducting Step 22.	
22	Tune the transceiver, in turn, to: Band 1: 1.6000 MHz mode 3 2.5000 MHz mode 3 4.4999 MHz mode 3 Band 2: 4.5000 MHz mode 3 6.5000 MHz mode 3 7.9999 MHz mode 3 Band 3: 8.0000 MHz mode 3 12.0000 MHz mode 3 14.9999 MHz mode 3 Band 4: 15.0000 MHz mode 3 25.0000 MHz mode 3 30.0000 MHz mode 3 5.0000 MHz mode 3	7 to 15 If 15 lit change to position K. 1 to 4 Lock LED lit throughout
23	Set transceiver rotary switch to OFF.	

Table 5.1.5 Test Routine 4 - Check Synthesiser (Contd)

Step	Action	Indication
24	Disconnect cables CX 2015 and 3513 171 3337.	
25	Reconnect coax cable disconnected at Step 17.	
26	Disconnect test unit and reconnect ribbon cables.	
27	Refer to Fig 5.1.3.	

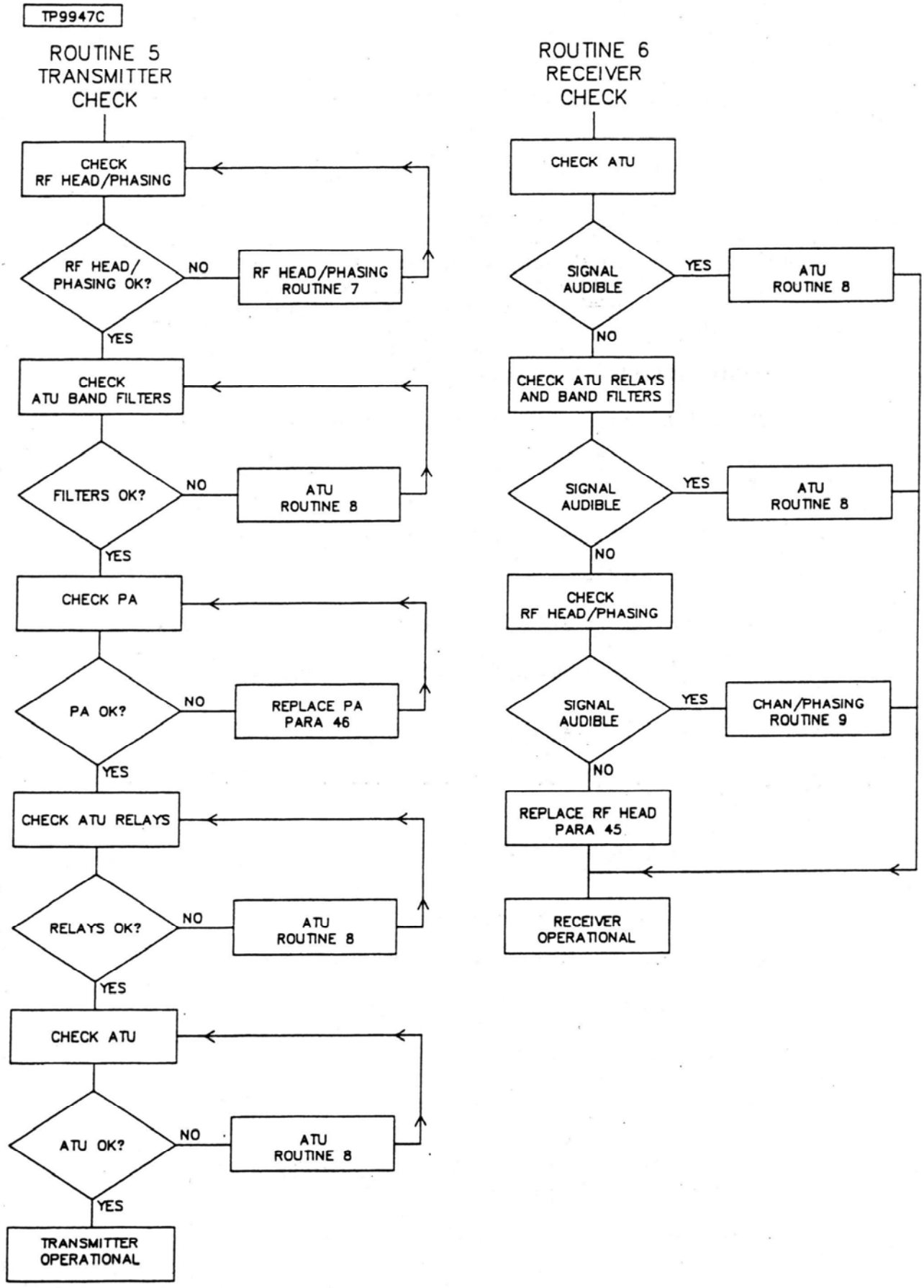


Fig 5.1.4 Transmitter and Receiver Checks - Flow Diagram

Test Routine 5 - Transmitter Check

27 Refer to Table 5.1.6 and Fig 5.1.3, 5.1.4 and 5.1.5. Fig 5.1.4 refers to Tables 5.1.8, 5.1.9 and 5.1.10.

Table 5.1.6 Test Routine 5 - Transmitter Check

Step	Action	Indication
	Note: If any indication is incorrect for any of the following series of tests, refer to Fig 5.1.4 for guidance at the conclusion of the appropriate test.	
	Transmitter Check - RF Head/Phasing	
1	Disconnect ATU coax cable from RF Head output	
2	Connect cable CX 2015 between test set and RF Head output.	
3	Set test set FUNCTION switch to position K.	
4	Set transceiver rotary switch to K/B.	
5	Tune transceiver to 5.6250 MHz, Mode 3.	
6	Operate handset pressel and hold while conducting Step 7.	
7	On test set, press the ON switch and monitor LED indication.	12 to 15
8	Release ON switch.	
9	Repeat steps 6 to 8 on modes 1, 2, 4 and 5 in turn and whistle into MIC.	1 to 15 (flashing)
10	Set transceiver rotary switch to OFF.	
11	Disconnect cable CX 2015 from RF Head output.	
12	Reconnect ATU coax cable to RF Head output.	
	Transmitter Check - ATU Band Filters	
13	Disconnect coax cable from PA input.	
14	Using a miniature coax cable from 3513 171 3337 (male/male) connect cable CX 2015 to connector of cable disconnected in Step 13.	
15	Set transceiver rotary switch to K/B.	

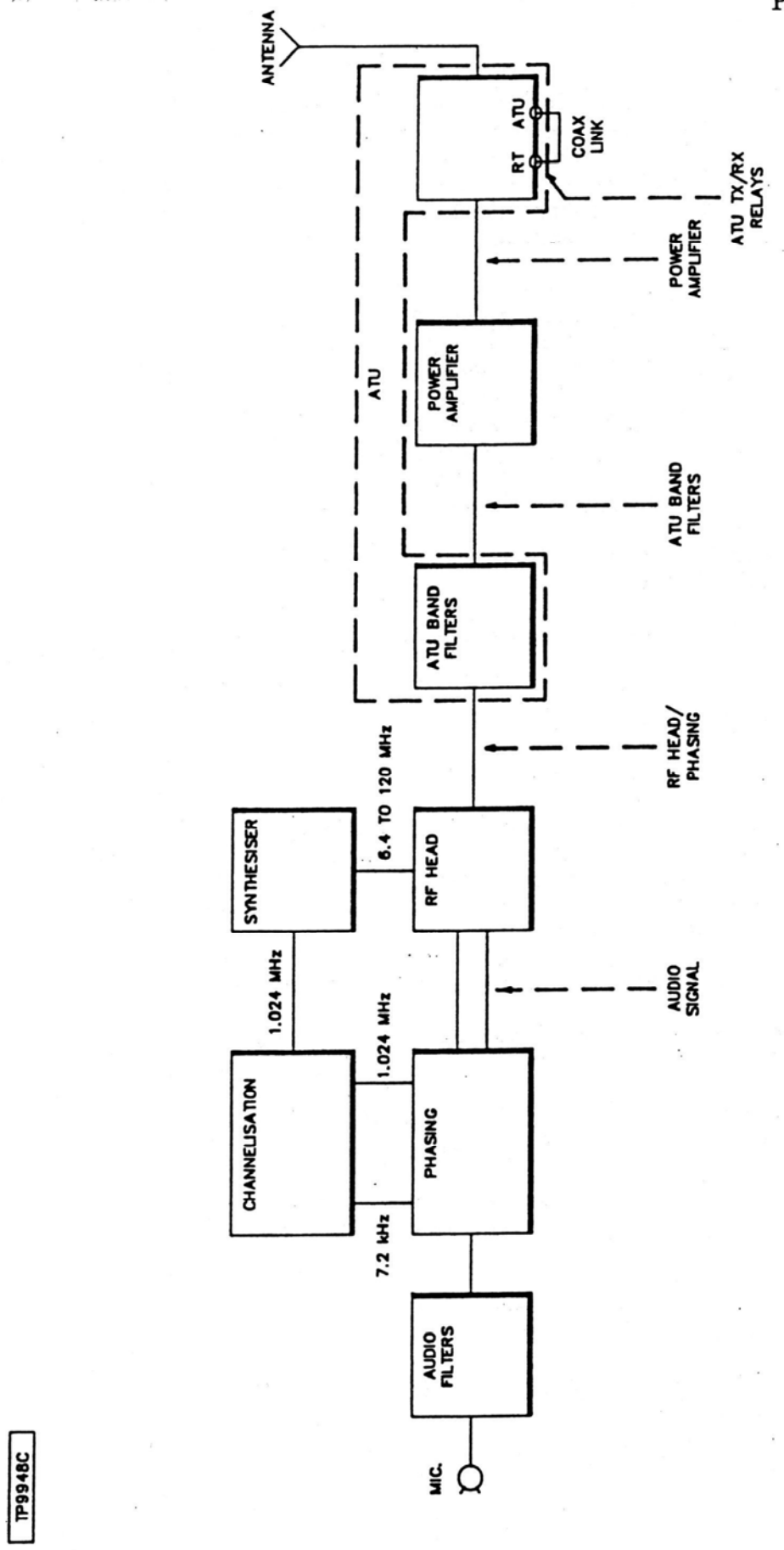


Fig 5.1.5 Simplified Transmit Path - Test Access Points

Table 5.1.6 Test Routine 5 - Transmitter Check (Contd)

Step	Action	Indication
16	For each of the following frequencies in turn, conduct operations 17 and 18. 1.8750 MHz, mode 3 2.5000 MHz, mode 3 3.7500 MHz, mode 3 5.6250 MHz, mode 3 9.3750 MHz, mode 3 13.1250 MHz, mode 3 16.2500 MHz, mode 3 25.6250 MHz, mode 3 29.3750 MHz, mode 3	
17	Operate and hold the handset pressel while conducting Step 18.	
18	On the test set, press the ON switch and monitor LED indication.	6 to 14
19	Release ON switch.	
20	Set transceiver rotary switch to OFF.	
21	Disconnect cables CX 2015 and 3513 171 3337	
22	Reconnect ATU coax cable to PA input.	
	Transmitter Check - PA **Note:** A battery **MUST** be used to perform this test.	
23	Connect cable CX 2010 to the Rx(HL)/Tx socket on the test set.	
24	Connect one end of cable CX 2015 to cable CX 2010 and the other end to the PA output connector.	
25	Remove the transceiver fuse and connect cable CX 2011 between the transceiver fuse holder and the test set.	
26	Using PA Supply Extension lead 3513 171 3338, connect the PA supply to the PA module.	
27	Connect Extension lead 3513 171 3336 between ATU and RF Head output.	
28	Set test set FUNCTION switch to position E.	
29	Set transceiver rotary switch to K/B.	
30	At the transceiver, select low power (4 watt)	

Table 5.1.6 Test Routine 5 - Transmitter Check (Contd)

Step	Action	Indication
31	Tune transceiver to each of the following frequencies in turn and conduct Steps 32 and 33. 1.8750 MHz mode 3 9.3750 MHz mode 3 29.3750 MHz mode 3	
32	Operate and hold the handset pressel while conducting Step 33.	
33	On test set, press the ON switch and monitor LED indication.	3 to 6
34	Release ON switch and pressel.	
35	Set test set FUNCTION switch to position G.	
36	Operate and hold the handset pressel while conducting Step 37, and monitor the handset earpiece.	1 KHz tone
37	On the test set press the ON switch and monitor LED indication.	1 to 3
38	Release ON switch and pressel.	
39	Set test set FUNCTION switch to position E.	
40	At the transceiver, select high power (20 watt).	
41	Repeat operations 31 to 37 observing LED indications as follows; Step 33 Step 37	 11 to 14 7 to 11
42	Set transceiver rotary switch to OFF.	
43	Disconnect cable CX 2011 and re-insert fuse.	
44	Disconnect cable CX 2015.	
	Transmitter Check - ATU Tx/Rx Relays	
45	Connect cable CX 2010 to the RT socket on the transceiver front panel (remove coaxial 'U' link if fitted).	
46	Using miniature coax cable (male/female) 3513 171 3336, connect the output of the PA to the ATU.	

Table 5.1.6 Test Routine 5 - Transmitter Check (Contd).

Step	Action	Indication
47	Set test set FUNCTION switch to position E.	
48	Set transceiver rotary switch to K/B.	
49	Ensure high power (20 watt) is still selected at the transceiver.	
50	Tune transceiver to 5.6250 MHz mode 3.	
51	Operate and hold handset pressel while conducting Step 52.	
52	On test set, press the ON switch and monitor LED indication.	11 to 14
53	Release ON switch and pressel.	
54	Set transceiver rotary switch to OFF.	
55	Disconnect cable CX 2010 from RT socket.	
	Transmitter Checks - ATU Tuning	
56	Connect coaxial 'U' link between RT and ATU sockets on the transceiver front panel.	
57	Connect the dummy antenna BA 1343 to the antenna screw socket on the transceiver front panel and connect the earth braid to the front panel earthing terminal.	
58	Connect cable CX 2010 to the BNC connector on the end of the dummy antenna.	
59	Set test set FUNCTION switch to position E.	
60	Set transceiver rotary switch to K/B.	
61	At the transceiver select high power (20 watt).	
62	Tune transceiver to 1.8750 MHz mode 3 and listen for operation of the ATU coarse tune motor.	ATU Motor
63	Operate and hold the handset pressel and listen for operation of the ATU fine tune motor.	ATU Motor
64	While holding the handset pressel, on the test set press the ON switch and monitor LED indication	1 or greater

Table 5.1.6 Test Routine 5 - Transmitter Check (Contd)

Step	Action	Indication
65	Repeat Steps 62 to 64 for the following frequencies	
	2.5000 MHz, Mode 3	1 to 7
	3.7500 MHz, Mode 3	3 to 8
	5.6250 MHz, Mode 3	3 to 9
	9.3750 MHz, Mode 3	4 to 11
	13.1250 MHz, Mode 3	5 to 11
	16.2500 MHz, Mode 3	6 to 11
	25.6250 MHz, Mode 3	7 to 12
	29.3750 MHz, Mode 3	7 to 12
66	Set transceiver rotary switch to OFF.	
67	Disconnect extension cables 3513 171 3336 and 3513 171 3338.	
68	Disconnect cable CX 2010.	
69	Remove dummy load.	

Test Routine 6 - Receiver Check

28 Refer to Table 5.1.7 and Fig 5.1.3, 5.1.4, 5.1.6 and 5.1.9. Fig 5.1.4 refers to Tables 5.1.8, 5.1.9 and 5.1.10.

Table 5.1.7 Test Routine 6 - Receiver Check

Step	Action	Indication
	Note: If any indication is incorrect for any of the following series of tests, refer to Fig 5.1.4 for guidance at the conclusion of the appropriate test.	
	Receiver Check - RT Socket/ATU	
1	Connect cable CX 2010 between test set socket Rx(LL) and the RT socket on the transceiver front panel (if necessary remove ATU/RT 'U' link).	
2	Connect cable CX 2014 between test set and the AUDIO 1 socket on the transceiver front panel.	
3	Using miniature coax cables (male/female) (2 off) 3513 171 3336, connect the output of the PA to the ATU and the output of the RF Head to the ATU.	
4	Set test set FUNCTION switch to position B.	
5	Set transceiver rotary switch to K/B.	
6	Using Memory Store Key BA 1233, store the following data in the channels indicated:	

Channel	Frequency	Mode
0	5.0000 MHz	8
1	1.8750 MHz	8
2	2.5000 MHz	8
3	3.7500 MHz	8
4	5.6250 MHz	8
5	9.3750 MHz	8
6	13.1250 MHz	8
7	16.2500 MHz	8
8	25.6250 MHz	8
9	29.3750 MHz	8

7	Disconnect Memory Store Key and connect handset to AUDIO 2.	
8	Select channel 1 at transceiver and listen for noise of mechanical band changing.	
9	Adjust transceiver for maximum volume at keyboard.	

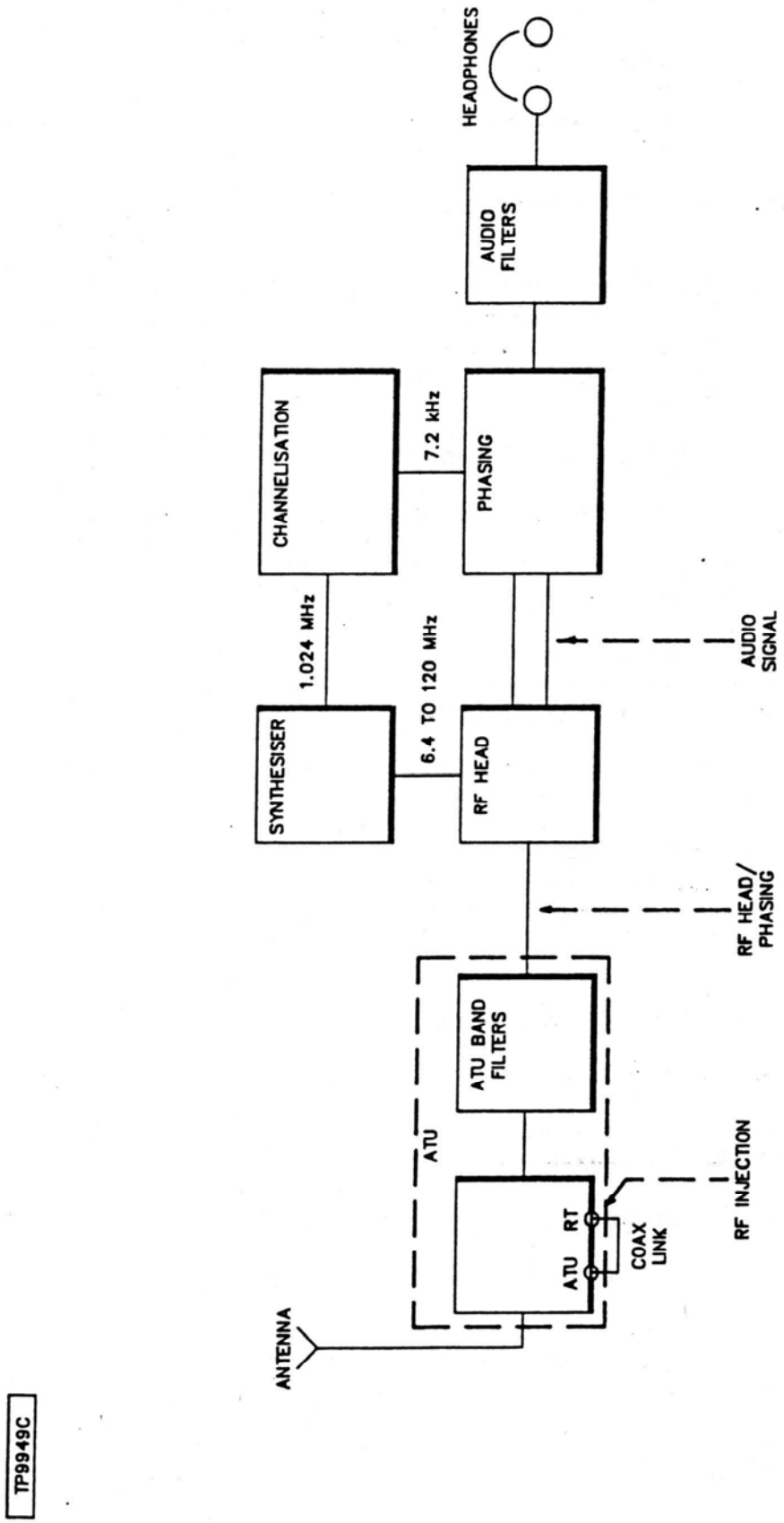


Fig 5.1.6 Simplified Receiver Path - Test Access Points

Table 5.1.7 Test Routine 6 - Receiver Check (Contd)

Step	Action	Indication
10	At test set press and hold ON switch while conducting Steps 11 to 13.	
11	Listen for audio tone in the handset earpiece and monitor LED indication	1 kHz tone 12, 13, 14 or 15
12	At transceiver keyboard press and hold '-' key while monitoring audio tone in earpiece.	Tone decreases to inaudible
13	At transceiver keyboard press '+' key and hold until LED indicator 14 is lit.	
14	Set test set FUNCTION switch to position C.	
15	At test set press ON switch and monitor audio tone and LED indication.	2 to 7
16	Repeat Steps 8 to 15 for channels 2 to 9.	
17	Set transceiver rotary switch to OFF.	
	Receiver Check - ATU Relays/Band Filters	
18	Disconnect cable CX 2010 from the RT socket on the transceiver front panel.	
19	Disconnect miniature coax cable from RF Head and connect one end of cable CX 2015 in its place.	
20	Connect remaining end of cable CX 2015 to free end of cable CX 2010.	
21	Set test set FUNCTION switch to position B.	
22	Set transceiver rotary switch to K/B.	
23	Select channel 1 at transceiver and listen for noise of mechanical band changing.	
24	Adjust transceiver for maximum volume at keyboard.	
25	At test set press and hold ON switch while conducting Steps 26 to 28.	
26	Listen for audio tone in the handset earpiece and monitor LED indication	1 kHz tone 12, 13, 14 or 15
27	At transceiver keyboard press and hold '-' key while monitoring audio tone in earpiece.	Tone decreases to inaudible
28	At transceiver keyboard press '+' key and hold until LED indicator 14 is lit.	

Table 5.1.7 Test Routine 6 - Receiver Check (Contd)

Step	Action	Indication
29	Set test set FUNCTION switch to position C.	
30	At test set press ON switch and monitor audio tone and LED indication.	2 to 7
31	Repeat Steps 23 to 30 for channels 2 to 9.	
32	Set transceiver rotary switch to OFF.	
	Receiver Check - RF Head/Phasing	
33	Insert the ATU/Phasing Test Connector BA 1341 (Fig 5.1.9 item f) between the Phasing and the RF Head ribbon connector.	
34	Disconnect handset from AUDIO 2 socket and connect to AF Adaptor BA 1342.	
35	Connect AF adaptor blue lead to test connector pin 20 (0 V) and red lead to pin 18 (AF Rx Chan 1).	
36	Disconnect cable CX 2010 from test set socket Rx(LL) and reconnect to socket Rx(HL)/Tx.	
37	Set test set FUNCTION switch to position B.	
38	Set transceiver rotary switch to K/B.	
39	Tune transceiver to 5.0000 MHz, Mode 8.	
40	At test set press ON switch and hold while conducting Steps 41 and 42.	
41	Monitor audio tone at handset.	1 kHz tone
42	At transceiver keyboard press '1'; press '-' eight times monitoring the audio tone at the handset.	Tone decreases to inaudible
43	Set transceiver rotary switch to OFF.	
44	Transfer AF adaptor red lead to test connector pin 19 (AF Rx Chan 2).	
45	Repeat Steps 38 to 42.	
46	Set transceiver rotary switch to OFF.	
47	Disconnect all test cables, adaptors, and the BA 1341 Test Connector.	
48	Refer to Fig 5.1.3	

Test Routine 7 - RF Head/Phasing

29 Entry to this test routine is accomplished from test routine 5, refer to Fig 5.1.4. The routine is written to continue from the particular exit point of routine 5 with minimum setting-up, and is not intended to be a self contained test.

30 This test routine is detailed in Table 5.1.8 and refers to Fig 5.1.4, 5.1.5 and 5.1.9.

Table 5.1.8 Test Routine 7 - RF Head/Phasing

Step	Action	Indication
1	Using miniature coax cable 3513 171 3336, connect the RF Head to the ATU.	
2	Insert ATU/Phasing Test Connector BA 1341 (Fig 5.1.9 item F) between the Phasing and the RF Head ribbon connector.	
3	Connect cable CX 2013 to test set.	
4	Connect handset to AUDIO 2 socket.	
5	Using pin adaptors connect the black lead of CX 2013 to pin 1 (0 V) of the test connector and the red lead, in turn, to each of the pins indicated in Step 9.	
6	Set test set FUNCTION switch to position A.	
7	Set transceiver rotary switch to K/B.	
8	Tune transceiver to 5.0000 MHz, mode 3.	
9	At test set, press the ON switch and hold throughout the following sequence; monitor LED indication	
	Pin 2 (+12 V)	11
	Pin 3 (+5 V)	4
	Pin 4 (-6 V) reverse connections	5
	Pin 5 (Tx protect)	0
	Pin 7 (Low/High power) - Low power	4
	High power	0
	Pin 8 (Tx/Rx 1) - Rx	0
	Tx - operate pressel	4
	Pin 9 (Dc mode) operate pressel	4
	(modes 1,2,4 and 5) operate pressel	0
	Pin 10 (Tx/Rx 2) - Rx	0
	Tx - operate pressel	4
	Pin 13 (0 V)	0
	Pin 16 (0 V)	0
	Pin 17 (0 V)	0
	Pin 20 (0 V)	0

Table 5.1.8 Test Routine 7 - RF Head/Phasing (Contd)

Step	Action	Indication
10	Set transceiver rotary switch to OFF.	
11	Connect CX 2013 red lead to Pin 12 (AGC).	
12	Connect cable CX 2010 between the test set Rx(HL)/ Tx socket and the transceiver RT socket.	
13	Set test set FUNCTION switch to position B.	
14	Set transceiver rotary switch to K/B.	
15	At the test set press and hold the ON switch while conducting Step 16.	
16	Set test set FUNCTION switch to position A and monitor LED indication.	LEDs 1 to 3 lit very briefly
17	Set transceiver rotary switch to OFF.	
18	Disconnect cable CX 2013.	
19	Disconnect handset from AUDIO 2 socket and connect to AF Adaptor BA 1342.	
20	Connect AF Adaptor blue lead to test connector Pin 16 (0 V) and red lead to Pin 14 (AF Tx Chan 2).	
21	Set transceiver rotary switch to K/B.	
22	Press 'CALL' key and monitor audio tone in handset earpiece.	2 seconds of two tone
23	Transfer AF adaptor red lead to pin 15 (AF Tx Chan 1).	
24	Press 'CALL' key and monitor audio tone in handset earpiece.	2 seconds of two tone
25	Transfer AF adaptor blue lead to Pin 20 (0 V) and red lead to Pin 18 (AF Rx Chan 1).	
26	Set test set FUNCTION switch to position B.	
27	Check transmitter tuned to 5.0000 MHz, Mode 3 (Channnel 0).	
28	At test set press the ON switch and hold while conducting Steps 29 and 30.	
29	Monitor audio tone at handset.	1 kHz tone

Table 5.1.8 Test Routine 7 - RF Head/Phasing (Contd)

Step	Action	Indication
30	At the transceiver keyboard press '1'; press '-' eight times monitoring the audio tone at the handset.	Audio decreases to inaudible
31	Transfer AF Adaptor red lead to pin 19 (AF Rx Chan 2).	
32	At test set press and hold ON pushbutton throughout Step 32; monitor audio tone at handset.	No audio tone
33	At the transceiver keyboard press '+' eight times while monitoring the audio tone at the handset.	Audio tone increases to maximum
34	Set transceiver rotary switch to OFF.	
35	Disconnect AF adaptor from test connector and from handset.	
36	Reconnect handset to AUDIO 2 socket.	
37	Disconnect cable CX 2010 on the test set and RT socket. **Note:** If indications are correct, replace the RF Head as detailed in para 46 and continue at Step 44. If indications are incorrect continue directly at Step 38.	
38	Disconnect the RF Head ribbon connector from the test connector.	
39	Using pin adaptors connect the black lead of CX 2013 to pin 1 (0 V) of the test connector and the red lead, in turn, to each of the pins indicated in Step 41.	
40	Set test set Function switch to position A.	
41	Set transceiver rotary switch to K/B.	
42	At test set, press the ON switch and hold throughout the following sequence; monitor LED indication.	
	Pin 2 (+12 V)	11
	Pin 3 (+5 V)	4
	Pin 4 (-6 V) reverse connections	5
	Pin 5 (Tx protect)	0
	Pin 7 (Low/High power) - Low power	4
	High power	0

Table 5.1.8 Test Routine 7 - RF Head/Phasing (Contd)

Step	Action	Indication
	Pin 13 (0 V) Pin 16 (0 V) Pin 17 (0 V) Pin 20 (0 V)	0 0 0 0
43	Set transceiver rotary switch to OFF. **Note:** If the indications are not correct, change the Phasing as detailed at para 50 before continuing at Step 44. If indications are correct continue directly at Step 44.	
44	Remove ATU/Phasing Test Connector and remake ribbon connection.	
45	Disconnect cable CX 2013.	
46	Disconnect miniature coax cable 3513 171 3336.	
47	Refer to Fig 5.1.4.	

Test Routine 8 - ATU

31 Entry to this test routine is accomplished from either test routine 5 or test routine 6; see Fig 5.1.4. The routine is written to continue from the particular exit point of the referal routine with minimum setting-up, and is not intended to be a self contained test.

32 This test routine is detailed in Table 5.1.9 and refers to Fig 5.1.4 and 5.1.8.

Table 5.1.9 Test Routine 8 - ATU

Step	Action	Indication
1	Insert the ATU/Phasing Test Connector BA 1341 (Fig 5.1.8 item L) between the ATU Assembly and the ATU ribbon connector.	
2	Connect cable CX 2013 to the test set.	
3	Connect 'U' link between RT and ATU sockets on the transceiver front panel.	
4	Screw dummy antenna into antenna socket and connect earth braid to chassis earth terminal.	
5	Set test set FUNCTION switch to position A.	
6	Set transceiver rotary switch to K/B.	
7	Tune transceiver to 1.8750 MHz mode 3.	
8	Set transceiver volume to maximum at keyboard.	
9	At test set press ON switch as necessary to obtain LED indication while conducting the remaining Steps.	
10	Connect cable CX 2013 black lead to test connector Pin 18 (0 V) and red conector as directed in Steps 11 to 24.	
11	Connect red lead to Pin 1 (retune); press in turn 'CANCEL', 'STORE', 'CALL' and monitor LED indication and handset earpiece.	4 Continuous tone followed by two tone.
12	Connect red lead to Pin 2 (manual reverse); press in turn 'TUNE', '+' and monitor LED indication.	4 No LED lit while '+' pressed
13	Connect red lead to Pin 3 (Tx protect). Press 'CANCEL' and monitor LED indication.	0
14	Connect red lead to Pin 4 (Band select; select channel 2 at transceiver and monitor LED indication. Reselect channel 1.	4 No LED lit while band changing

Table 5.1.9 Test Routine 8 - ATU (Contd)

Step	Action	Indication
15	Connect red lead to Pin 5 (Rx protect/Tx inhibit) and monitor LED indication.	0
16	Connect red lead to Pin 6 (Amp Control) and monitor LED indication.	11
17	Connect red lead to Pin 7 (manual forward); press in turn 'TUNE', '-' and monitor LED indication.	4 No LED lit while '-' pressed
18	Connect red lead to Pin 8 (RF CW Demand). Press 'CANCEL', select Mode 3 then press 'CALL' and monitor LED indication.	4 No LED lit while tuning
19	Connect red lead to Pin 9 (Tx/Rx1); monitor LED indications and listen for relay click as transmit pressel is operated.	4 (Rx) 0 (Tx)
20	For each of the following frequencies in turn monitor LED indication at pins 10, 11, 12 and 13.	PIN 10 11 12 13
	1.8750 MHz Mode 3	4 0 0 0
	2.5000 MHz Mode 3	0 4 0 0
	3.7500 MHz Mode 3	4 4 0 0
	5.6250 MHz Mode 3	0 0 4 0
	9.3750 MHz Mode 3	4 0 4 0
	13.1250 MHz Mode 3	0 4 4 0
	16.2500 MHz Mode 3	4 4 4 0
	25.6250 MHz Mode 3	0 0 0 4
	29.3750 MHz Mode 3	4 0 0 4
21	Connect the red lead to each of the following pins and monitor LED indication.	
	Pin 14 (+5 V)	4
	Pin 15 (+12 V)	11
	Pin 16 (Battery +ve switched)	14 or 15
22	Connect cable CX 2010 between dummy antenna connector and test set connector Rx(HL)/Tx.	
23	Connect red lead to Pin 19 (Reverse Power); select low power at keyboard, operate pressel and monitor LED indication.	0 to 3
24	Connect red lead to Pin 20 (Forward Power); operate pressel and monitor LED indication.	3 to 5
25	Set transceiver rotary switch to OFF.	
	Note: 1. If results are correct proceed to Step 30.	
	2. If results are not correct continue at Step 26.	

Table 5.1.9 Test Routine 8 - ATU (Contd)

Step	Action	Indication
26	Disconnect ATU ribbon connector from the test connector.	
27	Set transceiver rotary switch to K/B.	
28	Repeat Steps 11 to 24 observing the following results.	

Step	Pin	Observation
11	1	4 no retune possible
12	2	4 no retune control
13	3	0
14	4	0
15	5	0
16	6	0
17	7	4 no manual control
18	8	0
19	9	4
20	10,11,12,13	As previously
21	14,15,16	As previously
22	-	-
23	19	0
24	20	0

29	Set transceiver rotary switch to OFF.	
	Note: 1. If indications are correct replace the ATU as detailed in para 50 and continue at Step 30.	
	2. If indications are incorrect replace the Channelisation as detailed in para 48 and repeat test routine 8.	
30	Disconnect cable CX 2010.	
31	Remove dummy antenna.	
32	Disconnect cable CX 2013.	
33	Remove ATU/Phasing Test Connector and remake ribbon connection.	
34	Refer to Fig 5.1.4.	

Test Routine 9 - Channelisation/Phasing

33 Entry to this routine is accomplished from test routine 6; see Fig 5.1.4. The routine is written to continue from the exit point of routine 6 with minimum setting-up, and is not intended to be a self contained test.

34 This test routine is detailed in Table 5.1.10 and refers to Fig 5.1.4 and 5.1.9.

Table 5.1.10 Routine 9 - Channelisation/Phasing

Step	Action	Indication
1	Insert the Channelisation/Phasing Connector BA 1340 (Fig 5.1.9 item 0).	
2	Connect RF Head to the ATU assembly using miniature coax cable 3513 171 3336.	
3	Disconnect the RT/ATU 'U' link at the transceiver front panel.	
4	Transfer handset from AUDIO 2 to AUDIO 1.	
5	Connect cable CX 2013 to the test set.	
6	Set test set FUNCTION switch to position A.	
7	Set transceiver rotary switch to K/B.	
8	Tune transceiver to 5.0000 MHz mode 3.	
9	At test set press ON switch as necessary to obtain LED indication while conducting the following Steps.	
10	Connect cable CX 2013 black lead to pin 3 (0 V) of test connector, and red lead as directed in Steps 11 to 21.	
11	Connect red lead to each of the following pins in turn and monitor LED indication.	
	Pin 1 (+12 V)	11
	Pin 2 (-6 V) connections reversed	5
	Pin 4 (+5 V)	4
	Pin 5 (0 V)	No LED lit
	Pin 6 (+6 V AGC)	5
	Pin 7 (+6 V)	5
12	Connect cable CX 2010 between test set connector Rx(HL)/Tx and transceiver RT socket.	
13	Set test set FUNCTION switch to position B.	
14	At test set press ON switch and monitor audio tone at handset.	1 kHz tone

Table 5.1.10 Routine 9 - Channelisation/Phasing (Contd)

Step	Action	Indication
15	With red lead connected to pin 8 (AGC Display), set test set FUNCTION switch to position A.	3, for a few seconds
16	Connect red lead to each of the following pins in turn and monitor LED indication.	
	Pin 9 (1.024 MHz clock)	0
	Pin 35 (1.024 MHz clock)	4
	Pin 10 (0 V)	0
	Pin 11 (7.2 kHz)	0
	Pin 36 (7.2 kHz)	4
17	Set test set FUNCTION switch to position B.	
18	At test set press ON switch and monitor audio tone at handset.	1 kHz tone
19	With red lead connected to pin 12, set test set FUNCTION switch to position A.	3, for a few seconds
20	Connect red lead to each of the following pins in turn and monitor LED indication.	
	Pin 13 (Low/High) Power: Low	4
	High	0
	Pin 14 (Tx/Rx 1): Tx - operate pressel	4
	Rx	0
	Pin 15 (Tx protect)	0
	Pin 17 (Tx Mod) : Tx Mode 3) operate	4 - tone
	Tx Modes 1, 2, 4 and 5) pressel	0
	Pin 18 (Tx/Rx 2): Tx - operate pressel	4
	Rx	0
	Pin 19 (Tx/Rx 3): Tx Mode 3 - operate pressel	0 - tone
	Rx	0
	CALL Mode 3	4 - tone
	Tx Modes 1, 2, 4 and 5 - operate pressel	4
	Pin 20 (Inhibit): Rx mode 3	0
	Tx mode 3 - operate pressel	4
	Pin 21 (LSB/USB): Modes 0, 2, 5 and 7	4
	Modes 1, 3, 4, 6, 8 and 9	0
	Pin 23 (Speech Processing): Modes 1,2,3,6,7 and 8	4
	Modes 4,5,9 and 0	0
	Pin 24 (Speech Processing): Modes 1,2,3,6,7 and 8	4
	Modes 4,5,9 and 0	0
	Pin 25 (Mic 2): Rx mode 3	0
	Tx mode 3 - operate pressel	0
	CALL mode 3	0
	Tx modes 1,2,4 and 5 - operate	4
	Pin 26 (Key 1) pressel	1

Table 5.1.10 Routine 9 - Channelisation/Phasing (Contd)

Step	Action	Indication
	Pin 27 (Mic 1) handset AUDIO 2: Rx mode 3	0
	Tx mode 3 - operate pressel	0
	CALL mode 3	0
	Tx modes 1,2,4 & 5 - operate pressel	4
	Pin 28 (Ch/PR2) handset AUDIO 2	4
	handset AUDIO 1: Rx	1 to 3
	Tx - operate pressel	0
	Pin 29 (Intercom) Push 'IC'	4
	Push 'CANCEL'	0
	Pin 30 (Volume Control) Push '-' minimum	1
	Push '+' maximum	9
	Push '-' normal	4 or 5
	Pin 31 (Full remote Programme Key):	
	BA 1233 Memory Store key in AUDIO 2	0
	Remove key	1
	Pin 32 (CALL) Push 'CALL'	3 or 4
	Pin 33 (Ch/PR1) handset AUDIO 2: Rx	1 to 4
	Tx - operate pressel	0
	Pin 34 (Sidetone and Alarm): Rx	0
	Tx mode 3	3 or 4 - tone
	Tx modes 1,2,4 and 5	0
21	Set transceiver rotary switch to OFF.	
	Note: 1. If results are correct proceed to Step 24	
	2. If results are not correct proceed to Step 22.	
22	Disconnect test connector from Phasing PEC.	
23	Repeat Steps 11 to 21; test on Pins 8 and 12 are not applicable.	
	Note: 1. When transmit mode is required connect a shorting link across pin 28 to 33 to pin 5 or 10 (0 V), or push CALL if applicable to particular test.	
	2. If indications are correct replace Phasing PEC as detailed at para 49 and repeat routine 9.	
	3. If indications are not correct replace channelisation as detailed at para 48 and repeat routine 9.	
24	Disconnect test connector BA 1340.	

Table 5.1.10 Routine 9 - Channelisation/Phasing (Contd)

Step	Action	Indication
25	Disconnect cable 3513 171 3336.	
26	Disconnect cable CX 2013.	
27	Disconnect cable CX 2010.	
28	Transfer handset to AUDIO 2.	
29	Refer to Fig 5.1.4.	

SUB-ASSEMBLY AND PEC REMOVAL AND REPLACEMENT

Location and Identification of Parts

35 The location, identity and area designation of RT 2000 assemblies and PECs are shown in Fig 5.1.10.

Sequence of Operations

36 The battery may be removed with the set closed. The desiccant may be removed with the set closed or with the set open. For all other operations the lid assemblies must be open. Assemblies/PECs may be serviced in any order.

Battery

37 To remove the battery, proceed as follows:

(1) Stand the set on the front panel.

(2) Release four spring clips and remove the battery compartment cover.

(3) Use the webbing handle to remove the battery.

(4) Check pin alignment and replace by reverse procedure.

Desiccant Removal - Set Closed

38 To remove the desiccant container with the set closed, proceed as follows:

(1) Lay the set on the Upper Lid Assembly.

(2) Identify the desiccant plug by reference to Fig 5.1.10.

(3) Unscrew the desiccant plug using the desiccant plug extractor tool.

(4) Unscrew the desiccant container from the plug.

(5) Replace by reverse procedure.

(6) Tighten the plug to a torque of 2.0 to 2.2 Nm.

Desiccant Removal - Set Open

39 With the Lower Lid Assembly open (para 40), the desiccant container may be renewed by unscrewing it from the plug by hand without disturbing the plug.

CAUTION: TO AVOID DAMAGE TO RIBBON CONNECTORS ALWAYS USE THE RIBBON CONNECTOR EXTRACTOR TOOL.

Upper Lid Assembly

40 To open the Upper Lid Assembly, proceed as follows:

(1) Stand the set on its lefthand side.

(2) Remove twelve M3 x 8mm socket head screws and sealing washers and one M4 socket head screw to free the lid assembly.

(3) Hinge the lid down to lay flat.

41 To remove the Upper Lid Assembly from the Case Assembly, proceed as follows:

(1) Disconnect the coaxial connector from the RF Head.

(2) Release the four screws to free the lid of the PSU.

(3) Disconnect the ribbon connector from the Synthesiser.

(4) Disconnect the ribbon connector from the PSU.

(5) Remove three outgoing wires from the PSU terminal block. Connections are shown in Table 5.1.11.

(6) Release the two flexible hinge straps at their point of attachment to the case.

Note: Before reclosing the lid apply Aeroshell 6 grease to the rubber nitrile lid seal.

(7) Replace by reverse procedure.

Table 5.1.11 PSU Terminal Block Connections

Colour	No Off	Connection
Brown	1	TB1-1
Black	1	TB1-2
White	1	TB1-3

Lower Lid Assembly

42 To open the Lower Lid Assembly, proceed as follows:

(1) Stand the set on its lefthand side

(2) Remove twelve M3 x 8mm socket head screws and sealing washers and one M4 socket head screw to free the lid assembly.

(3) Hinge the lid partially down.

(4) Disconnect two coaxial connectors and the supply connector from the Power Amplifier (PA) assembly.

(5) Disconnect the coaxial connector from the RF Head and allow the Lower Lid Assembly to hinge fully down to lie flat.

43 To remove the Lower Lid Assembly from the Case Assembly, proceed as follows:

(1) From the RF Head disconnect the ribbon connector between this item and Phasing.

(2) From the Case Assembly disconnect the coaxial connector joining this item to the RF Head.

(3) Release the two flexible hinge straps at their point of attachment to the case.

Note: Before reclosing the lid apply Aeroshell 6 grease to the rubber nitrile lid seal.

(4) Replace by reverse procedure.

PSU

44 To remove the PSU from the Upper Lid Assembly, proceed as follows:

(1) Open the Upper Lid Assembly as detailed in para 40.

(2) Release four screws and remove lid of PSU.

(3) Disconnect ribbon connector from Channelisation.

(4) Disconnect three wires from PSU terminal block (Table 5.1.11).

(5) Remove four M2.5 hexagonal spacers and washers to release the PEC.

(6) Replace by reverse procedure.

Synthesiser

45 To remove the Synthesiser from the Upper Lid Assembly, proceed as follows:

(1) Open the Upper Lid Assembly as detailed in para 40.

(2) Disconnect coax connector from RF Head.

(3) Disconnect ribbon connector from Synthesiser.

(4) Remove four M2.5 x 5mm pan head screws and washers and take off lid.

(5) Remove five M2.5 x 5mm pan head screws and washers.

(6) Swing out top PEC and remove six M2.5 hexagonal spacers to release the PEC.

(7) Replace by reverse procedure.

RF Head

46 To remove the RF Head from the Lower Lid Assembly, proceed as follows:

(1) Open Lower Lid Assembly as detailed in para 42.

(2) From the RF Head disconnect the ribbon connector between this item and Phasing.

(3) From the Case Assembly disconnect the coaxial connector joining this item to the RF Head.

(4) Remove six M3 x 6 mm pan head screws and take away lid.

(5) Disconnect the ribbon connector from the RF Head to the PA.

(6) Disconect coaxial lead from Phasing.

(7) Remove six hexagonal spacers and washers to release the PEC.

(8) Replace by reverse procedure.

Power Amplifier

47 To remove the Power Amplifier from the Lower Lid Assembly, proceed as follows:

(1) Open Lower Lid Assembly as detailed in para 42.

(2) From the RF Head disconnect the ribbon connector between this item and Phasing.

(3) From the Case Assembly disconnect the coaxial connector joining this item to the RF Head.

(4) Remove six M3 x 6 mm pan head screws and take away lid.

(5) Disconnect the ribbon connector from the RF Head to the PA.

(6) Remove four M2.5 x 5 mm pan head screws and washers and take off lid.

(7) Remove two nylon screws from the heat sink assemblies at the end of the PEC.

(8) Detach the thermistor sensor from the power transistor fixing screw at the outer edge of the PEC.

(9) Remove three M2.5 x 5 mm and two M2.5 x 6 mm screws and crinkle washers to free the power transistors from the lid assembly.

(10) Remove four M2.5 x 5 mm spacers and washers to release the PEC.

(11) Replace by reverse procedure.

(12) The transistor securing screws removed in (7) should initially be finger tight and then torqued to 0.7 Nm.

(13) Ensure good thermal contact between the thermistor and the power transistor fixing screw.

AF Filter

48 To remove the AF Filter from the Case Assembly, proceed as follows:

(1) Remove the nut from each of the front panel audio sockets.

(2) Open Lower Lid Assembly as detailed in para 42.

(3) Remove two M3 cheesehead screws to free the AF Filter from the Case Assembly.

(4) From Phasing disconnect the ribbon connector which joins this item to the AF Filter.

(5) Record the disposition of the two wires on the AF Filter terminal block and disconnect.

(6) Remove the PEC by manipulating the audio sockets through the front panel. Take care not to damage the film wiring. Retain the two sealing rings.

(7) Before replacing the sealing rings lightly apply XG271 grease.

(8) Replace by reverse procedure.

Channelisation and Display

49 To remove Channelisation and the Display from the Case Assembly, proceed as follows:

(1) Open Upper Lid Assembly as detailed in para 40.

(2) Disconnect the coaxial connector from Channelisation.

(3) Release the four screws to free the lid of the PSU.

(4) Disconnect the ribbon connector from the Synthesiser.

(5) Disconnect the ribbon connector from the PSU.

(6) Disconnect all the ribbon connectors from Channelisation.

Note: To disconnect the connector between Channelisation and Phasing it will be found helpful to tilt the case slightly, away from the lid.

(7) Disconnect the ribbon connector from the Display.

(8) Remove six M2.5 x 6 mm and two M2.5 x 10 mm pan head screws and crinkle washers to release the two PECs.

(9) Replace by reverse procedure.

Phasing

50 To remove Phasing from the Case Assembly, proceed as follows:

(1) Open Lower Lid Assembly as detailed in para 42.

(2) Remove M2.5 x 10 mm screws, washers and mica insulation to free from the case assembly the two power transistors mounted on the front edge of Phasing.

(3) Disconnect all the ribbon connectors from Phasing.

(4) Remove eight M2.5 x 5 mm pan head screws and washers to release the PEC.

(5) Replace by reverse procedure.

ATU

51 To remove the ATU from the Case Assembly, proceed as follows:

(1) Open Upper Lid Assembly as detailed in para 40.

(2) Open Lower Lid Assembly as detailed in para 41.

(3) Record the disposition of the thick red and blue power supply leads on TB1 pins 1 and 2 of the ATU on the terminal strip at the rear of the case assembly. Disconnect these leads.

(4) Disconnect the two leads from the terminal strip at the front end of the ATU. Note the disposition of the leads.

(5) Disconnect the coaxial and ribbon connectors from the ATU.

(6) Unsolder the pink lead from the Coil Assembly to the antenna socket.

(7) Record the disposition of the two coaxial connectors from the RT and ATU sockets. Use long-nosed pliers to disconnect the connectors.

(8) Remove six M3 x 6mm pan head screws and crinkle washers to free the ATU.

(9) Remove one 7mm hexagonal pillar and screw.

(10) Withdraw the ATU from the top side of the Case Assembly taking care not to foul adjacent wiring.

(11) Replace by reverse procedure.

Input Protection

52 To remove the Input Protection from the Case Assembly, proceed as follows:

(1) Open the Upper Lid Assembly as detailed in para 40.

(2) Open the Lower Lid Assembly as detailed in para 42.

(3) Remove the ATU as detailed in para 51.

(4) Remove the M2.5 x 6mm screw which secures the PEC.

(5) Withdraw the PEC from its recess complete with wiring.

(6) Replace by reverse procedure.

Antenna Socket

53 To remove the antenna socket insulating block and toroidal seal from the case assembly proceed as follows:

(1) Remove Input Protection as detailed in para 52.

(2) Remove the M4 x 6mm hexagonal head screw and washers and the M8 nut and washers from the rear of the antenna socket insulating block.

(3) Withdraw the insulating block and toroidal seal.

(4) Replace by reverse procedure.

LEAK AND DRYING OFF CHECKS

Leak Testing Procedure

54 The equipment required to leak test the Transceiver consists of a means by which the unit can be pressurised, to a predetermined pressure, with air and a tank of water in which the Transceiver can be immersed.

55 The exact method of testing will depend on the leak test equipment availability, but in general, the following sequence of operation should be observed.

(1) Check the security of the screws of the unit-under-test (UUT). If necessary, tighten the UUT screws to the correct torque.

(2) Connect an air supply to the UUT by removing the desiccator (para 38) and replacing it with the pressurising adaptor MC 50106 (para 4.3).

(3) Pressurise the UUT to 4.5 psi (0.3 Bar).

(4) Immerse the UUT fully in the water.

(5) Ensure that all trapped air is released and brush away air bubbles attached to the surface of the UUT.

(6) Check that no rising air bubbles are observed for a period of two minutes of immersion, otherwise correct and retest.

(7) Depressurise the UUT and remove it from the water.

(8) Remove the pressurising adaptor MC 50106.

(9) Carry out the drying off procedure as detailed in para 56.

Drying Off Procedure

56 To dry off the UUT, proceed as follows:

(1) First remove any excess water on the UUT, using a low pressure air-line.

(2) Ensure the desiccator is **NOT** fitted

(3) Place the UUT in a suitable oven for two hours, set to a temperature of 52 ±3° C (126 ±5° F).

(4) Remove the UUT from the oven and place it into a vacuum chamber.

(5) Reduce the pressure in the vacuum chamber to 13 mBar (10 ton) for 60 minutes, after which time the pressure may be allowed to return to normal atmospheric pressure by venting dry nitrogen into the vacuum chamber.

Note: If a vacuum chamber is not available the unit may be flushed with dry nitrogen by introducing the gas through the desiccator aperture, after removing the venting bung. The gas should be allowed to flow for at least a minute before the bung and the desiccator are fitted.

(6) Remove the UUT from the vacuum chamber and immediatly fit a dry desiccator as detailed in para 38(5).

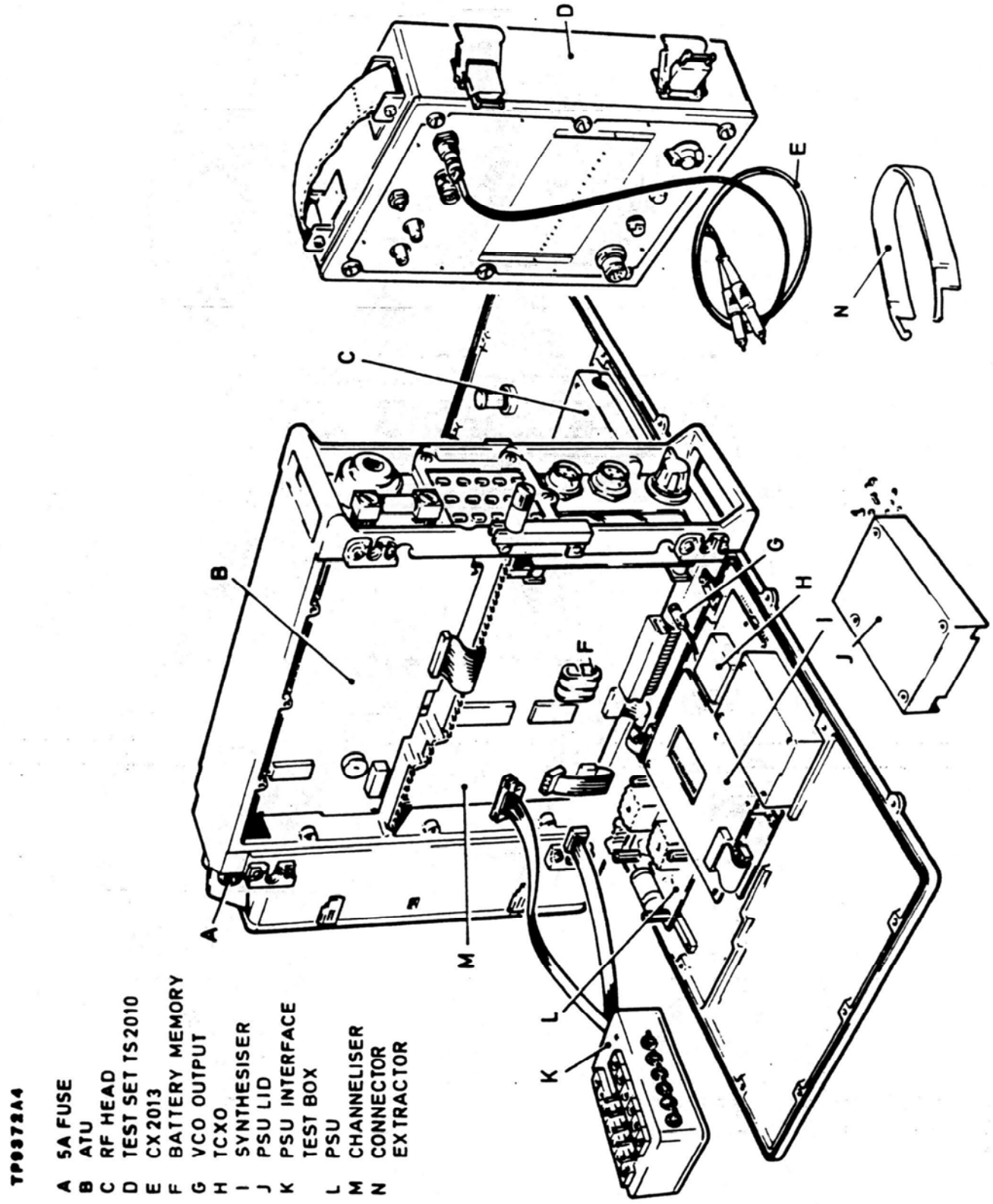


Fig 5.1.7 RT 2000 Test Configuration - PSU PEC

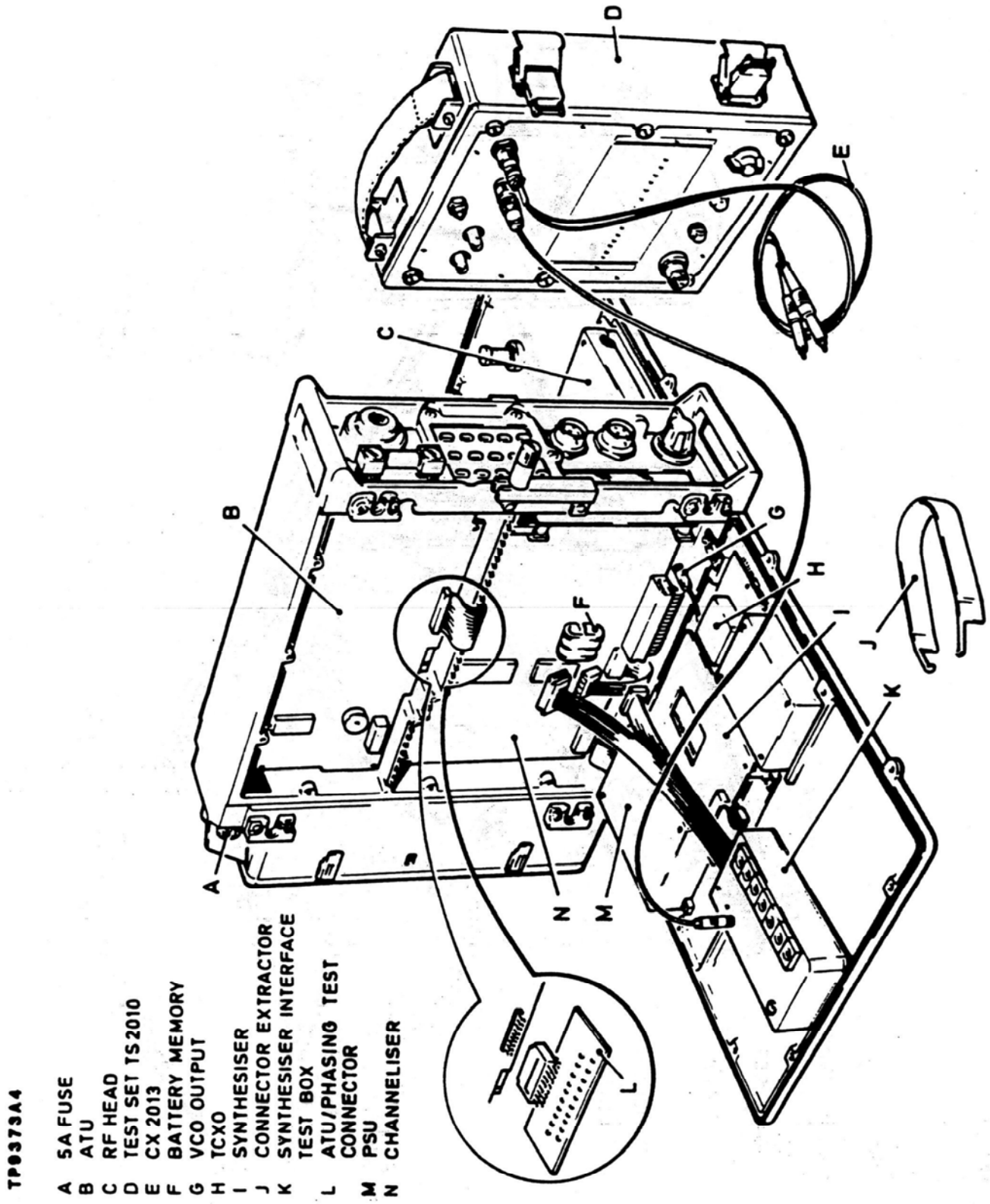


Fig 5.1.8 RT 2000 Test Configuration - Synthesiser

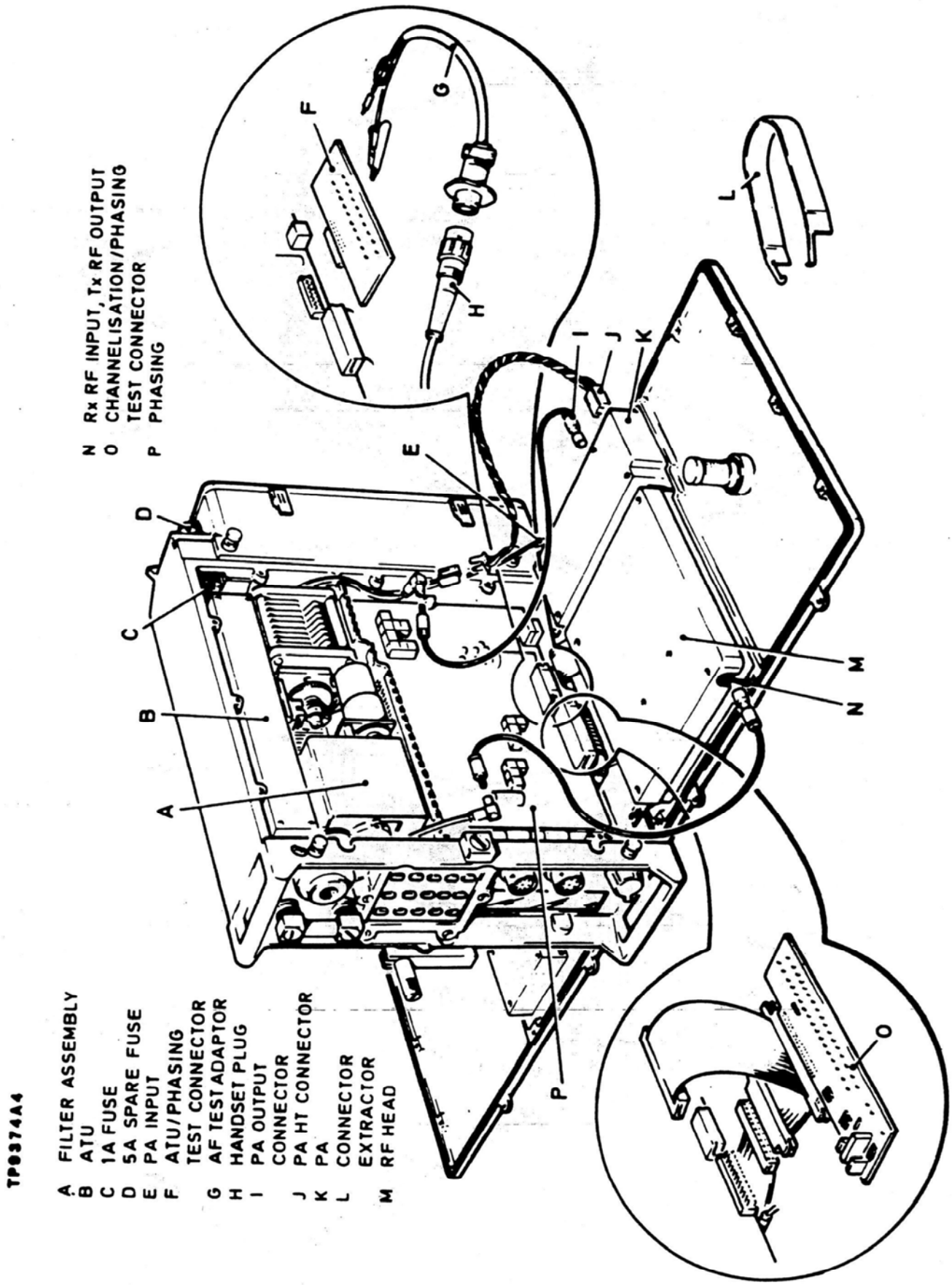


Fig 5.1.9 RT 2000 Test Configuration - RF Signal Path and RF Head

TP8223A3

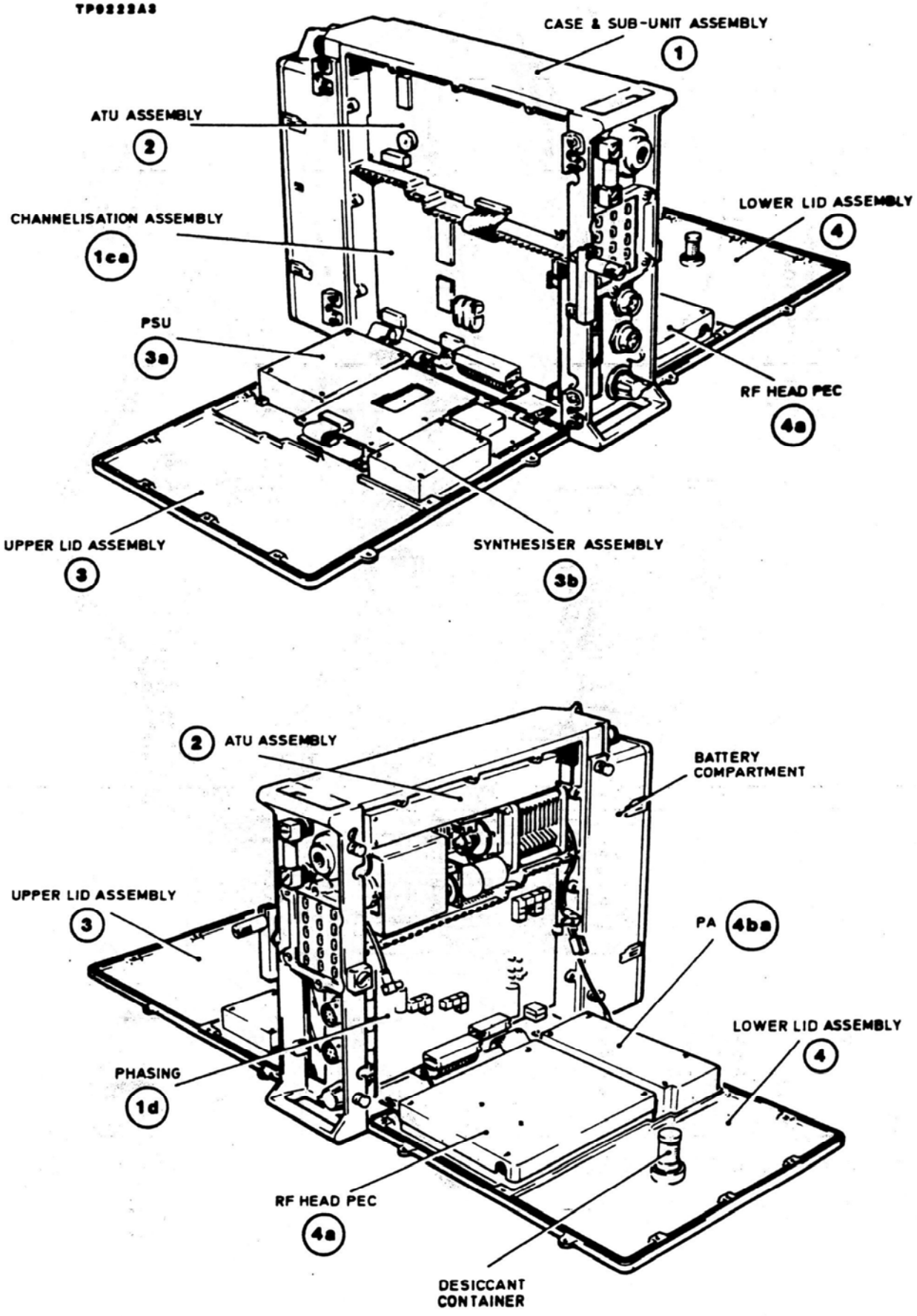


Fig 5.1.10 Assemblies/PEC Identification - BA 1172

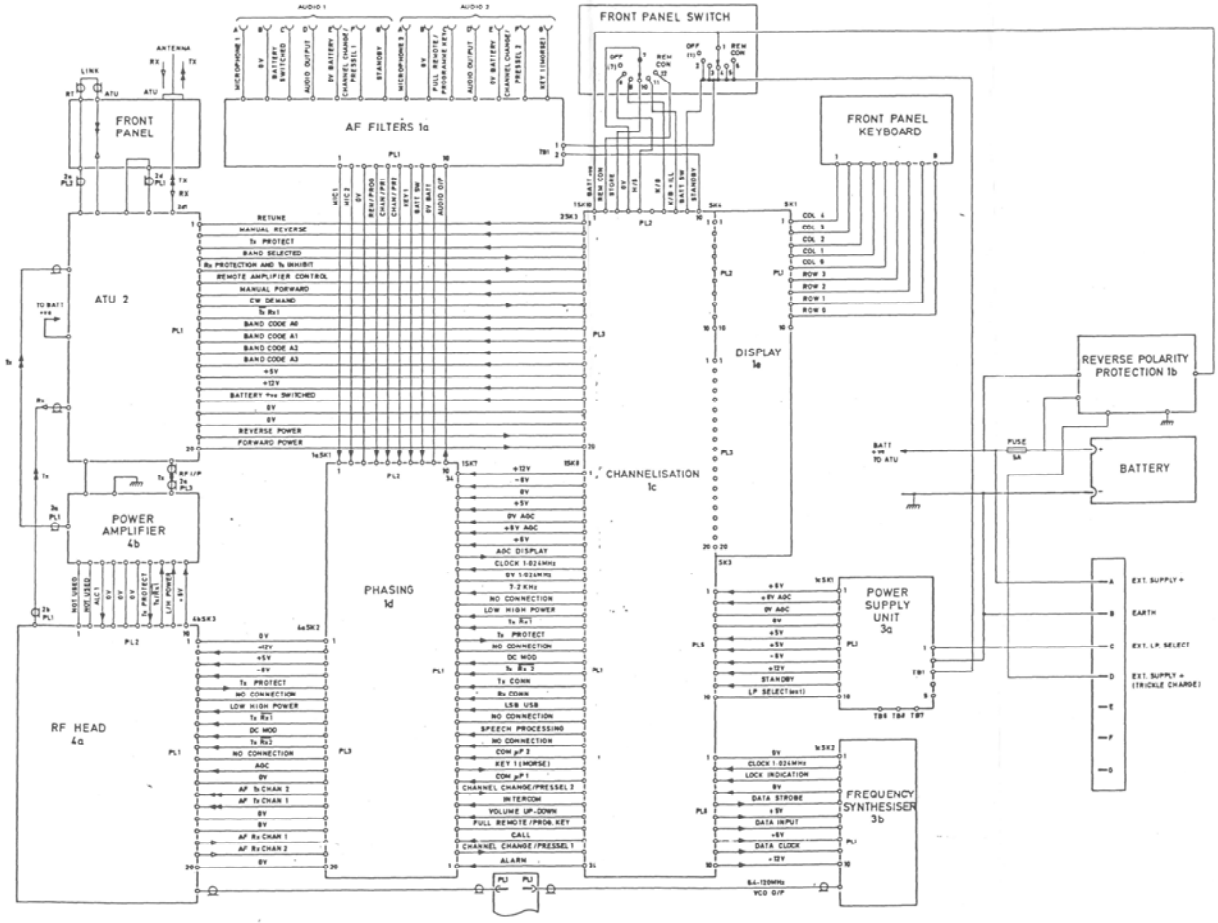


Fig 5.1.11 Interconnection Diagram - BA 1172 Fig 5.1.11

CATEGORY 7

PARTS CATALOGUE AND RELATED INFORMATION

Contents

Tables

CATEGORY 7

PARTS CATALOGUE AND RELATED INFORMATION

INTRODUCTION

1 Table 7.1 lists the items recommended for replacement at Level 2 (Second line) maintenance workshop.

Table 7.1 Schedule of Recommended Spares - Level 2

IPC Item	NOMENCLATURE	PART No.	No. Off
1-1	TRANSCEIVER GA BA 1172	9571 111 7200	Ref
1-2	Battery lid assembly	3513 160 6314	1
1-4	'0' seal 0041-16	2613 080 39221	4
1-7	Gasket	3513 151 1688	1
1-10	Cover (PSU)	3513 132 5142	1
1-11	Screw	2522 177 11037	4
1-12	Washer, crinkle	2513 712 06003	4
1-13	POWER SUPPLY UNIT PEC	3504 111 5847	1
1-17	Plug mounting assembly	3513 128 3972	1
1-18	Desiccant container	2813 060 08123	1
1-19	'0' seal 0196-24	2613 080 39202	1
1-20	Hinge strap	3513 132 5074	4
1-21	Screw	2522 177 11037	4
1-22	Washer, crinkle	2513 712 06003	4
11-1	CASE & SUB-UNIT ASSEMBLY (Area 1)	3513 172 2220	Ref
11-1a	Spacer, hexagonal	3513 128 4187	1
11-1b	Washer, crinkle	2513 712 06005	1
11-1c	Spacer, hexagonal	3513 128 4188	1
11-2	ATU ASSEMBLY	3513 172 1997	1
11-3	Washer, isolating	2413 490 90065	4
11-4	Bush, insulating	2413 490 90069	2
11-5	Screw	2522 177 11039	2
11-6	Washer, crinkle	2513 712 06003	2
11-7	PHASING PEC	3504 111 5853	1
11-8	CHANNELISATION PEC	3504 114 27840	1
11-9	DISPLAY PEC	3504 111 5849	1
11-10	Screw	2522 177 11038	8
11-11	Washer, crinkle	2513 712 06003	8
11-12	Cable assembly	3513 171 2937	1
11-15	Cable assembly	3513 171 2938	1
17-2	Screw	2522 177 11038	8
17-3	Washer, crinkle	2513 712 06003	8

Table 7.1 Schedule of Recommended Spares - Level 2 (Cont.)

IPC Item	NOMENCLATURE	PART No.	No. Off
19-1	CASE ASSEMBLY	3513 172 1998	Ref
19-3	Nut, knurled	3513 128 4291	1
19-12	Knob assembly	3513 172 1152	1
19-14	Screw with nylon insert	2513 200 14003	1
19-15	Nut, square	2513 500 05156	1
19-17	Clamp	3513 152 3152	1
19-18	Screw	3513 128 4299	6
19-19	Washer, crinkle	2513 712 06003	6
19-20	AF FILTER PEC	3513 147 4004	1
19-21	Screw	2522 177 11038	4
19-22	Washer, crinkle	2513 712 06003	4
19-37	Keyboard and gasket assembly	3513 020 6104	1
19-45	Link, BNC	3513 724 01728	1
19-46	Block, insulating	3513 151 1689	1
19-47	Screw	2522 032 55119	1
19-48	Washer, plain	2522 600 75026	1
19-49	Washer, crinkle	2513 712 06005	1
19-50	Nut, special	3513 128 4138	1
19-51	Washer, crinkle	2513 712 06008	1
19-52	Washer	3513 151 1744	1
19-53	Seal, toroidal	2613 080 39236	1
19-55	INPUT PROTECTION PEC	3513 147 2824	1
19-56	Nut	2522 401 20008	1
19-57	Washer, crinkle	2513 712 06004	1
19-69	Carrier, fuse	3513 151 9115	1
19-70	Screw	2522 187 06073	1
19-71	Fuse, 5A	3513 022 0335	1
19-72	Holder, fuse	2432 088 00019	1
19-73	Cover, electrical plug/socket	SD3/235131	1
18-2	Bracket, display	3513 152 3120	2
18-3	Screw	2522 177 11041	2
18-4	Screw	2522 177 11038	6
18-5	Washer, crinkle	2513 712 06003	8
18-6	Washer, isolating	2413 490 90065	2
12-1	ATU ASSEMBLY (Area 2)	3513 172 1997	1
12-2	Screw	2522 177 11059	6
12-3	Washer, crinkle	2513 712 06004	6
13-1	ATU PEC	3513 147 4054	Ref
13-70	Printed circuit connector 2-way	3513 022 0357	2
13-71	Printed circuit connector 4-way	3513 022 0358	2
3-1	UPPER LID ASSEMBLY (Area 3)	3513 172 4002	Ref
3-2	Screw] For use with	3513 128 4269	12
3-2a	Screw] Pressure Die Cast lid	3513 128 4270	1
	OR		

Table 7.1 Schedule of Recommended Spares - Level 2 (Cont.)

IPC Item	NOMENCLATURE	PART No.	No. Off
3-2	Screw]_ For use with	3513 128 4271	12
3-2a	Screw] Machined lid	3513 128 4272	1
3-3	Washer, sealing M3	2613 080 39219	12
3-3a	Washer, sealing M4	2613 080 39221	1
3-4	Cover (VCO)	3513 132 5140	1
3-5	Screw	2522 177 11037	4
3-6	Washer, crinkle	2513 712 06003	4
3-7	SYNTHESISER ASSEMBLY	3513 172 2178	1
2-1	POWER SUPPLY UNIT PEC	3504 111 5847	Ref
2-2	Spacer (PSU)	3513 128 3888	4
2-3	Washer, crinkle	2513 712 06003	4
4-2	Screw	2522 177 11037	1
4-3	Screw	2522 177 11038	2
4-4	Washer, crinkle	2513 712 06003	3
4-6	Spacer (Synthesiser)	3513 128 3886	3
4-7	Screw	2522 177 11037	3
4-8	Washer, crinkle	2513 712 06003	6
4-9	Spacer (VCO)	3513 128 3928	4
4-10	Washer, crinkle	2513 712 06003	4
7-1	LOWER LID ASSEMBLY (Area 4)	3513 172 4010	Ref
7-2	Screw)_ For use with	3513 128 4271	12
7-2a	Screw) Machined lid	3513 128 4272	1
	OR		
7-2	Screw)_ For use with	3513 128 4269	12
7-2a	Screw) Pressure Die Cast lid	3513 128 4270	1
7-3	Washer, sealing M3	2613 080 39219	12
7-3a	Washer, sealing M4	2613 080 39221	1
7-4	Screw	3513 128 4273	1
7-5	Seal	2613 080 98099	1
7-6	Lid, RF head, upper	4304 090 9983	1
7-7	Screw	2522 177 11038	6
7-8	Washer, crinkle	2513 712 06003	6
7-9	RF HEAD PEC	3504 111 5852	1
7-10	Spacer (RF head)	3513 128 3783	6
7-11	Lid, RF head, lower	4304 092 9904	1
7-11a	Spacer, thin (RF head)	3513 128 4194	6
7-12	PA/RF HEAD LID ASSEMBLY	3513 172 4006	1
8-2	Spacer (RF head)	3513 128 3931	6
8-3	Washer, crinkle	2513 712 06003	6
10-2	Spacer (PA)	3513 128 3889	4
10-3	Screw	2522 177 11038	3
10-4	Washer, crinkle	2513 712 06003	7
9-2	Cover (PA)	3513 132 5139	1
9-3	Screw	2522 177 11038	4

Table 7.1 Schedule of Recommended Spares - Level 2 (Cont.)

IPC Item	NOMENCLATURE	PART No.	No. Off
9-4	Washer, crinkle	2513 712 06003	11
9-5	Strip, insulating	3513 146 0314	1
9-6	Holder, resistor	3513 128 3986	1
9-7	Washer, crinkle	2513 712 06003	1
9-8	Screw	2522 177 11038	3
9-9	Washer, crinkle	2513 712 06003	3
9-10	POWER AMPLIFIER PEC	3504 111 5851	1
9-11	Bracket (PA)	3513 132 5165	1
9-12	Label, danger	3513 131 6365	1
	MATERIALS		Ref
62	Heat sink compound	1312 501 29501	
69	Adhesive	1322 511 24301	
60	Grease XG271	1313 501 23601	
	Grease Aeroshell 6		